Open ZR+ MSA

Technical Specification

Change History

REV No.	Date	Description
1.0	4-Sep-2020	First release publication – for 100 GHz grid spacing applications.
2.0	29-July-2022	Updated with parameters for 75 GHz grid spacing applications.

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Contents

1 Scope and Introduction

OpenZR+ defines specifications for 100-400G single-wavelength optical ports for transceiver/transponder, muxceiver/muxponder (TRXR/TRPN, MUXR/MUXP) node functions and for switch/router optical ports.

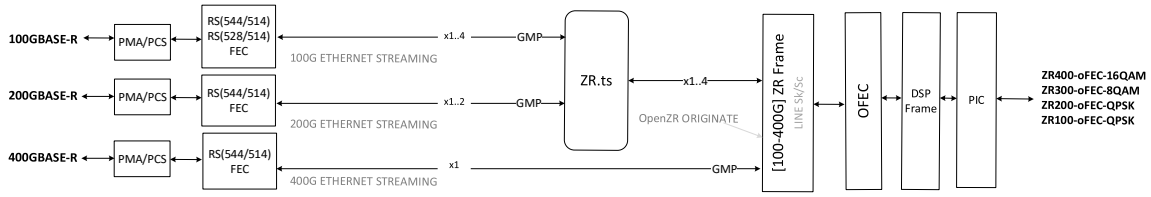


Figure 1-1: OpenZR+ Architecture reference

The architecture, shown in Figure 1-1 includes client sub-layers for up to four 100GBASE-R clients, up to two 200GBASE-R clients and a single 400GBASE-R client. Client data and alignment markers are extracted and re-timed to the line side clock domain using the general mapping protocol (GMP). Retimed data plus GMP timing information is then mapped into one of the OpenZR+ frame formats. Those frames are multiplexed and OFEC encoded and become the payload of a DSP frame with DP-16QAM, DP-8QAM, or DP-QPSK symbols.

Note: this specification makes no assumption about the allocation of functions on a line card or optical modules (albeit a typical module will provide a transceiver/muxceiver function for Ethernet signals 100G and beyond).

Table 1-1 lists possible combinations of clients and network lane interfaces included in this specification.

Table 1-1: Transceiver/Transponder (TRXR/TRXP) functions

OpenZR+ Format	Capacity	Host Lane Interfaces *			Network Lane Interface
		400G BASE-R	200G BASE-R	100G BASE-R	
400ZR+	400G	1	2	4	ZR400-OFEC-16QAM
300ZR+	300G			3	ZR300-OFEC-8QAM
200ZR+	200G		1	2	ZR200-OFEC-QPSK
100ZR+	100G			1	ZR100-OFEC-QPSK

* Only clients from one column may be multiplexed to a network interface, i.e., mixed modes are outside the scope of this specification.

OpenZR+ supports the combinations of network framing and modulation modes shown in Table 1-3.

Table 1-2: OpenZR+ Line Encoding, Modulation and Symbol Rates

OpenZR+ Format	SFF-8024 Media ID	Payload Rate	Framing Format	Symbol Baud Rate (+/- 20ppm)	Modulation	FEC	Net Coding Gain (NCG) (dB)	Pre-FEC BER	Reference Standard
400ZR+	46h	400G	ZR400-OFEC-16QAM	60 138 546 798	16QAM	OFEC	11.6	2.0E-2	OpenZR+
300ZR+	47h	300G	ZR300-OFEC-8QAM	60 138 546 798	8QAM				
200ZR+	48h	200G	ZR200-OFEC-QPSK	60 138 546 798	QPSK				
100ZR+	49h	100G	ZR100-OFEC-QPSK	30 069 273 399	QPSK				

1.1 400ZR+ Format

This DSP framing format is based on the OIF-ZR400-01.0 frame, adapted with open forward error correction (OFEC), then modulated over a dual polarization coherent interface with absolute (non-differential) 16QAM modulation. The payload can be of the following types:

- A single 400GBASE-R host interface GMP mapped into a clear channel ZR400 frame structure
- 2 × 200GBASE-R host interfaces each individually GMP mapped into a single channelized 400G ZR frame structure.
- 4 × 100GBASE-R host interfaces each individually GMP mapped into a single channelized 400G ZR frame structure.

1.2 300ZR+ Format

This DSP framing format is a reduced bandwidth 300G ZR frame, adapted with open forward error correction (OFEC), then modulated over a dual polarization coherent interface with absolute (non-differential) 8QAM modulation. The payload can be of the following type:

- 3 × 100GBASE-R host interfaces, each individually GMP mapped into a single channelized 300G ZR frame structure.

1.3 200ZR+ Format

This DSP framing format is a reduced bandwidth 200G ZR frame, adapted with open forward error correction (OFEC), then modulated over a dual polarization coherent interface with absolute (non-differential) QPSK modulation. The payload can be of the following types:

- A single 200GBASE-R host interface GMP mapped into a clear channel 200G ZR frame structure
- 2 × 100GBASE-R host interfaces, each individually GMP mapped into a single channelized 200G ZR frame structure.

1.4 100ZR+ Format

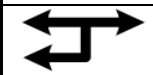
This DSP framing format is a reduced bandwidth ZR100 frame, adapted with open forward error correction (OFEC), then modulated over a dual polarization coherent interface with absolute (non-differential) QPSK modulation. The payload can be of the following types:

- A single 100GBASE-R host interface GMP mapped into a reduced rate 100G ZR frame structure

1.5 OpenZR+ Supported Client Modes

The combinations of host interfaces and media side interfaces listed in Table 1-3 may be supported by OpenZR+ implementations. Other modes of operation are possible but are vendor specific.

Table 1-3 Client modes supported by OpenZR+

Host Side	Datapath					Media Side
Host Interface	Host Map/Demap	MUX/DMUX	Media Framing	FEC Encode/Decode	Modulation	Media Interface
1 x 400GBASE-R	1 x 400ZR.ts		400ZR	OFEC	16QAM	ZR400-OFEC-16QAM
2 x 200GBASE-R	2 x 200ZR.ts					
4 x 100GBASE-R	4 x 100ZR.ts					
3 x 100GBASE-R	3 x 100ZR.ts		ZR300	OFEC	8QAM	ZR300-OFEC-8QAM
1 x 200GBASE-R	1 x 200ZR.ts		ZR200	OFEC	QPSK	ZR200-OFEC-QPSK
2 x 100GBASE-R	2 x 100ZR.ts					
1 x 100GBASE-R	1 x 100ZR.ts		ZR100	OFEC	QPSK	ZR100-OFEC-QPSK

2 OpenZR+ Block Diagram

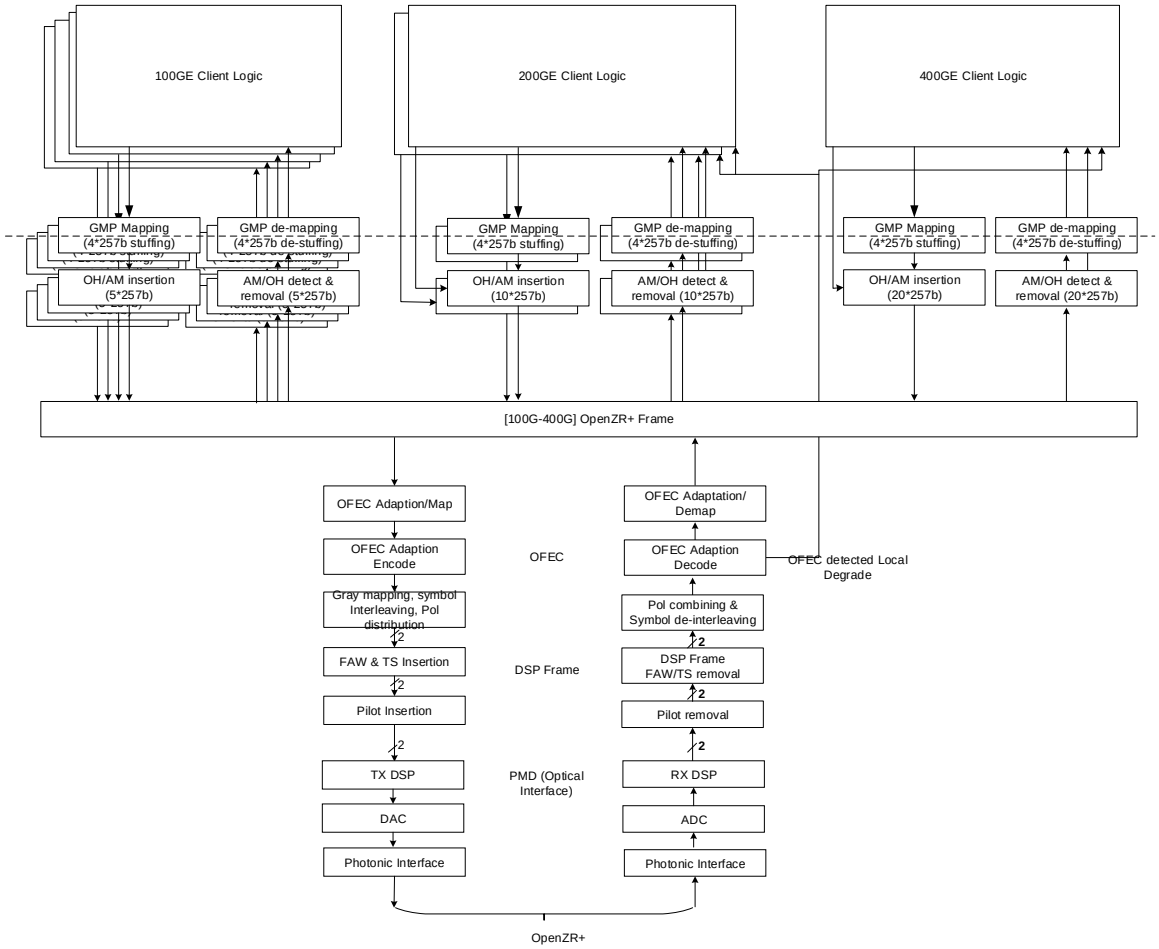


Figure 2-1 OpenZR+ Block Diagram

3 ZR frame structure

The ZR frame structure is defined prior to OFEC coder adaptation and OFEC processing. Aspects of the ZR frame structure that are specific to ZRx-OFEC-<modulation> are identified, otherwise the ZRx overhead is common to the requirements defined in OIF400ZR-01.0.

This section describes the various framing containers used in the ZR multiplexing / demultiplexing process. The generic ZRx frame/multi-frame structure is shown in.Figure 3-1. ZRx frames are based on the OIF 400ZR frame. Organized as m columns x n rows, with the values of m being either 5140 or 10280, and the values on n being 128, 192 or 256, all four ZRx frames are a multiple of 257 bits so that the 257-bit payloads fit into the designated payload area. Frame overhead bits are in the first row of each frame and include alignment markers (AM), pad (PAD), overhead (OH), and sufficient additional pad bits so that these overhead fields lie on a 257b boundary in the frame.

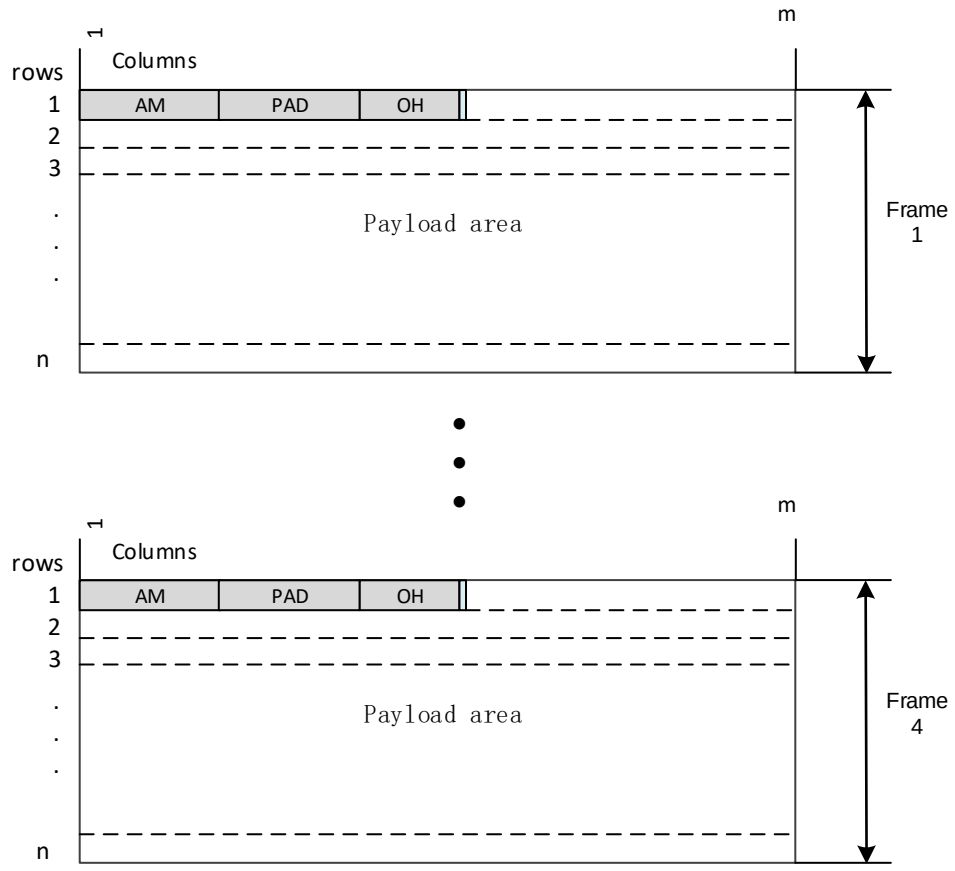


Figure 3-1 – Generic ZRx Frame and Multi-Frame structure

3.1 257-bit Blocks

The ZR frame payloads are broken down into 257-bit blocks. The number of 257-bit blocks is the same in all rows of the frame except the first row. The first row is shared with the AM/PAD/OH fields. Table 3-1 defines the number of 257-bit payload blocks for each of the various framing formats.

Table 3-1 – 257-bit blocks in ZRx frames and 4-frame multiframes

Server Mode	First row 257-bit blocks allocated to AM/PAD/OH and additional pad bits	Payload 257-bit blocks in 1 frame	Payload 257-bit blocks in 4 frames
ZR100	5	2555	10220
ZR200	10	5110	20440
ZR300	15	7665	30660
ZR400	20	10220	40880

3.2 ZR400 Frame

The diagrams in this section have been cloned directly from the 400ZR IA. Figure 3-2 shows the high-level format of the ZR400 frame without any FEC overhead. The frame is constructed using 256 rows of 10280 bits. Each row contains forty 257-bit blocks. The first twenty 257-bit blocks of the first row are used to support overhead information. The remaining (255*40) + 20 257-bit blocks are used for payload. There are sixteen frames in a multi-frame. The GMP algorithm is performed across a group of four consecutive frames.

The 400G frame provides 20 bits of padding between the OH area and the Payload area in order to insure both the OH and payload areas are multiples of 257-bit blocks. The 400G frame has 20 257-bit blocks of framing and 10220 257-bit blocks of payload. The 400G has four unique blocks of OH and each OH is 40 bytes in size.

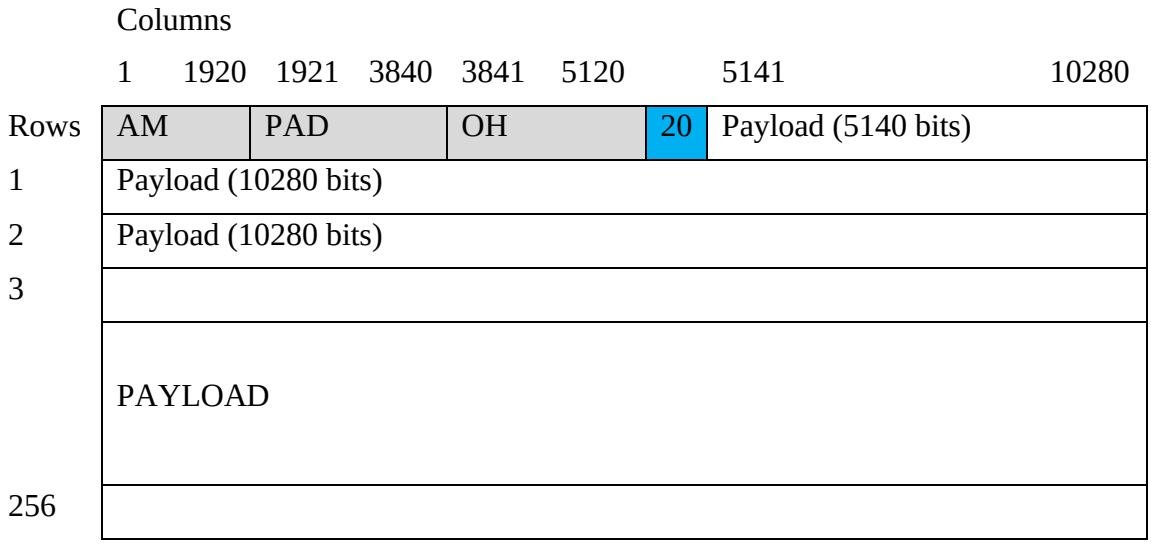


Figure 3-2 – 400G ZR400 Frame

3.3 ZR300 Frame

The 300G frame in Figure 3-3 differs slightly from the 400G frame.

- The 300G frame has 192 rows compared to 256 rows.

- The AM area contains 12 lanes of 120-bit alignment markers.
- The OH area contains 3 blocks of 320-bits instead of 4 blocks.
- The additional PAD between OH and payload is 15 bits.
- The 300G frame has AM/PAD/OH/additional pad bits in the first 3855 columns of the first row (corresponds to 15 x 257-bit blocks) and 7665x 257-bit blocks of payload.

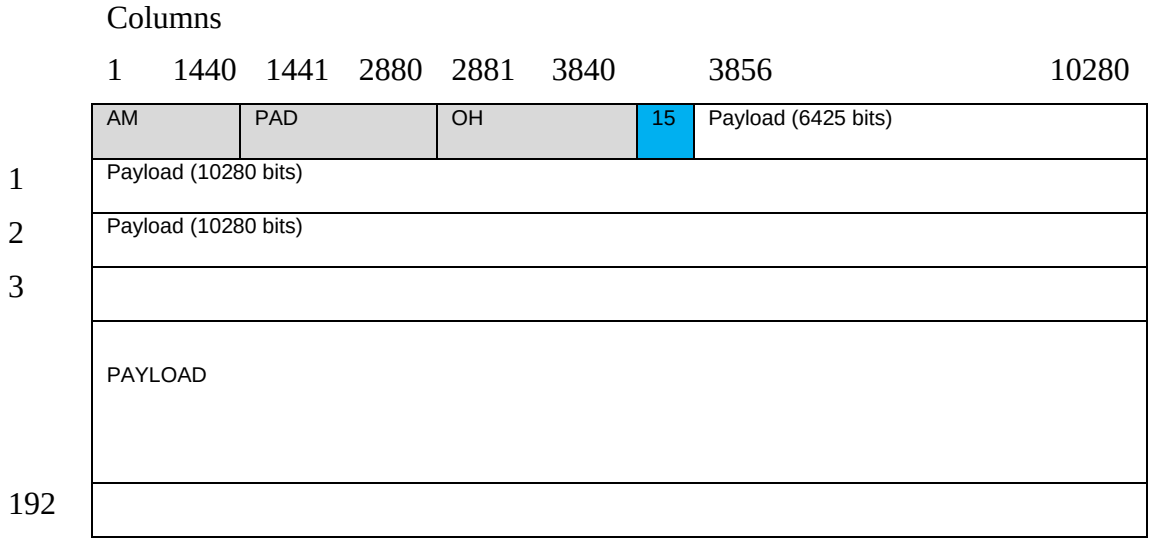


Figure 3-3 – ZR300 Frame

3.4 ZR200 Frame

The 200G frame in Figure 3-4 differs slightly from the 400G frame.

- The 200G frame has 128 rows compared to 256 rows.
- The AM area contains 8 lanes of 120-bit alignment markers
- The OH area contains 2 blocks of 320-bits instead of 4 blocks.
- The additional PAD between OH and payload is 10 bits.
- The ZR200 frame has AM/PAD/OH/additional pad bits in the first 2570 columns of the first row (corresponds to 10×257-bit blocks) and 5110×257-bit blocks of payload.

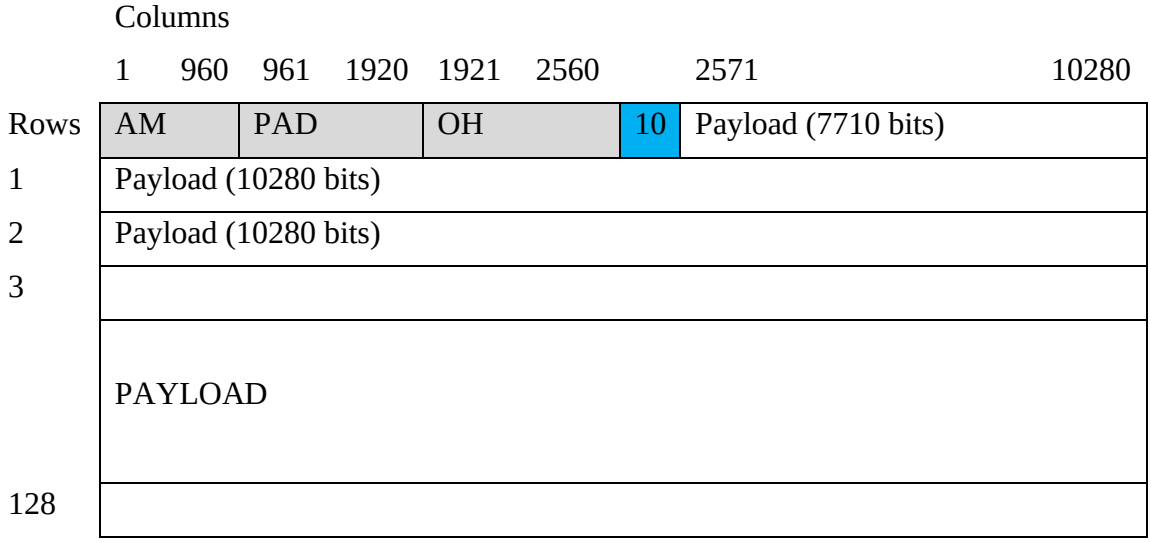


Figure 3-4 –ZR200 Frame

3.5 ZR100 Frame

The 100G frame in Figure 3-5 differs slightly from the 400G frame.

- The 100G frame has 128 rows compared to 256 rows.
- The 100G frame has 5140 bits per row compared to 10280 bits per row.
- The AM area contains 4 lanes of 120-bit alignment markers
- The OH area contains 1 block of 320-bits instead of 4 blocks.
- The additional PAD between OH and payload is 5 bits.
- The 100G frame has 5 257-bit blocks of OH and 2555 257-bit blocks of payload.

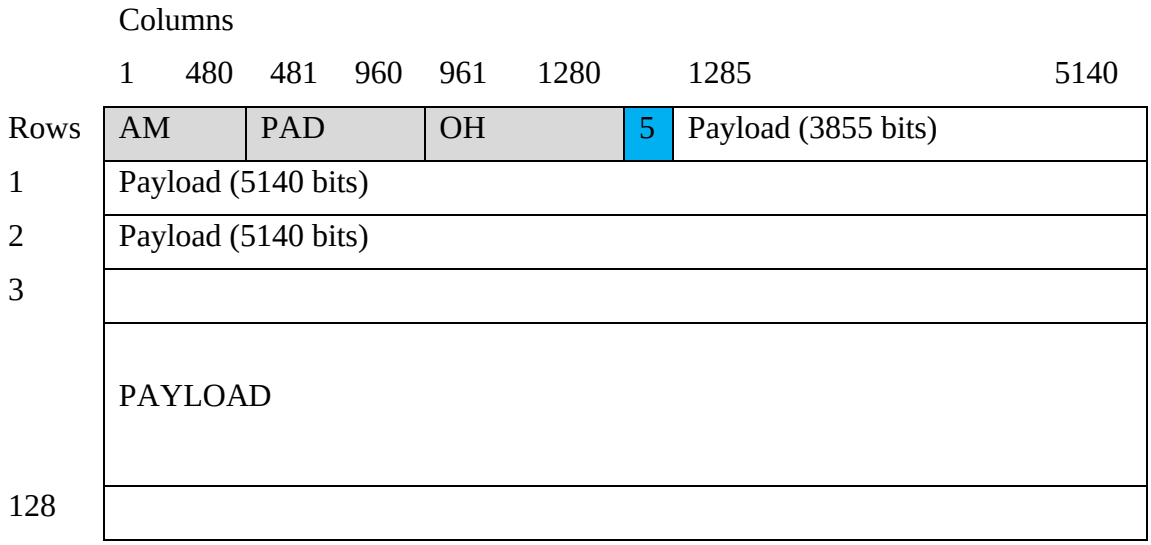


Figure 3-5 –ZR100 Frame

3.6 Framing Overhead

Figure 3-6 provides an expanded view of the framing area which is at the beginning of row 1. The AM section follows the recommendation defined in the 400ZR IA. The OH section follows the recommendation in OIF 400ZR IA. OpenZR+ also defines the Media Slot Identifier (MSI) byte.

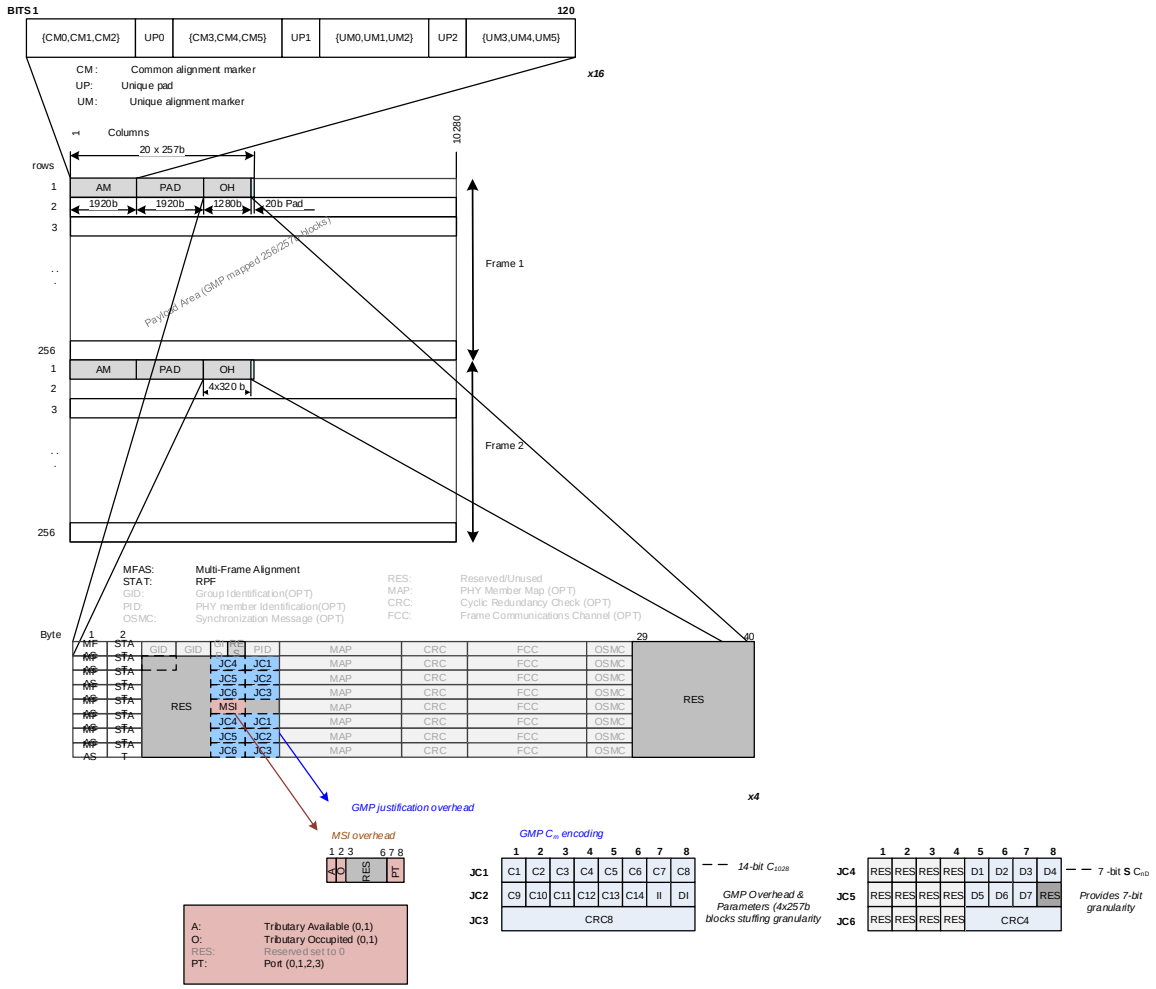


Figure 3-6 – ZR400 Framing (Overhead)

The ZR frame uses the STAT and GMP JC1-JC6 as defined in OIF 400ZR IA, and MFAS as defined in G.709. The ZR frame adds the additional MSI field. All other fields are optional or defined as OPT or RES.

3.7 Media Slot Identifier (MSI) / Tributary Slot Identifier (TSI)

- The Media Slot Identifier (MSI) in row 4, byte 5 follows the example of the PT22 MSI Byte as defined in G.709 Clause 20.4.1.1.
- OpenZR+ defines a 1:1 mapping between the host port and the Media Slot Identifier. These are then referred to as a Time Slot Instance TSI.
- Optionally a crossbar can be inserted between TSIs and the MSIs.
- The transmitter can send Cm/Cnd information in all OH locations, but the receiver must choose only one and the selection should be to choose Cm/Cnd from lowest ordinal OH assigned to the port.
- A port is assigned the number of tributaries required to accommodate the port rate.
- The tributaries are ordered in time with the lower ordinals first in time.
- The tributaries need not be consecutive to avoid bandwidth fragmentation.

Table 3-2 is an example of the MSI OH byte value for various configurations of a ZR400 frame.

MODE	OH1	OH2	OH3	OH4
1x400G	0xc0	0xc0	0xc0	0xc0
2x200G	0xc0	0xc0	0xc1	0xc1
4x100G	0xc3	0xc2	0xc1	0xc0

Table 3-2: MSI OH example values

4 Datapath Processing

For OpenZR+ applications the Tx data path maps and multiplexes up to four 100GBASE-R, two 200GBASE-R or one 400GBASE-R Host/Client signals into a channelized ZR container. Each channel is GMP mapped and 257b multiplexed into tributary unit(s) of a 200G, 300G, or 400G ZR frame structure. The 200-400G ZR frame overhead fields (AM, PAD, and OH) are partitioned in 10-bit tributary ordered slices. The ZR frame is then adapted with OpenFEC (OFEC). The higher coding gain of OFEC compared to CFEC as used for OIF 400ZR, enables support for metro, regional and long-haul reaches. It can also provide additional margin when operating on a 75 GHz grid.

The scope of this specification is how the node internal set of $n \times$ [100,200,400]GBASE-R signals are mapped into m *(m = [n/x])* ZR-x-OFEC-<modulation> signals, with each ZR-x signal containing "x" (frame/multi-frame aligned interleaved) ZR tributary mapped signals ($x \geq 1$).

The digital formatting and processing done by the ZR-x-OFEC-<modulation> port function is shown in Figure 4-1.

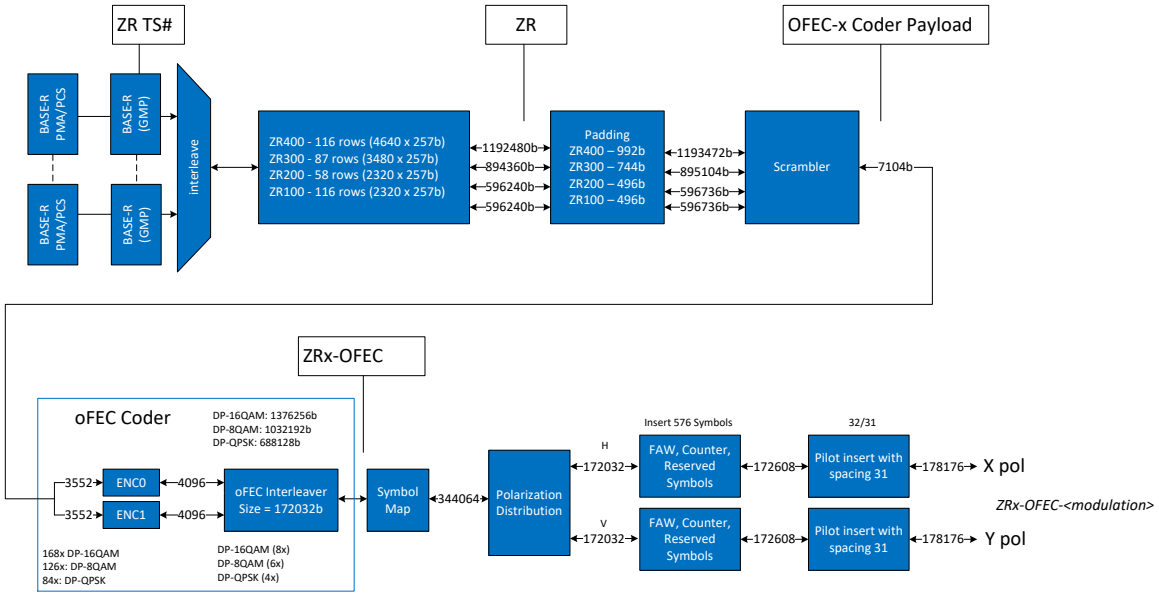


Figure 4-1: Digital port functions for a single ZRx-OFEC-mQAM signal

4.1 OpenZR+ Multiplexing/Demultiplexing (ZRMAP/ZRDEMAP)

OpenZR+ supports the mapping / de-mapping (ZRMAP/ZRDEMAP) and multiplexing / demultiplexing (ZRMUX/ZRDMUX) of up to 1 × 400GBASE-R, 1 or 2 × 200GBASE-R, or 1..4 × 100GBASE-R host interfaces. Combinations of 200GBASE-R and 100GBASE-R host interfaces are also feasible, but outside the scope of this specification release. The Ethernet host interfaces are assumed to be within +/-100ppm of each other, but otherwise asynchronously framed.

A high-level list of functions provided by OpenZR+ Muxceivers/Muxponders include:

- Multiplexing/Demultiplexing of Ethernet frames in 257-bit blocks.
- GMP mapping of Ethernet frames into n x 100G tributary slots.

- Reflection of PHY fault in reverse direction.
- Forward and reverse handling of LD, RD indicators, and local handling of FEC Degrade detection. ZR overhead information insertion/removal (MFAS, STAT, GID, PID, MSI, and GMP JC1-JC6).
- PRBS generation/checking for the ZR payload.
- Local Fault sourcing for tributary slots in alarm state.

4.2 GMP Definition

The ZR400 frames operate at a fixed server frequency. The server frequency is higher than what is required to carry the payload. The difference between the input payload and the payload capacity is handled using GMP stuffing blocks. The client traffic is mapped into the ZR400 payload using GMP blocks. The GMP processor calculates the number of active and stuffing GMP blocks for each frame. The active GMP blocks are filled with client traffic while the stuffing GMP blocks are filled with a fixed pattern of all zeros.

The GMP process is defined in G.709 Annex D.

4.3 GMP Blocks

A consecutive set of 257-blocks are combined to form a GMP block. The ZR400 frame supports multiplexing of n x 100G to 400G clients, up to the ZRx frame bandwidth.. Each client rate uses a different number of 257-bit blocks for each GMP block. The GMP algorithm is used across a period of four ZR400 frames. The number of GMP blocks for each client rate is shown in Table 4-1. All client rates have the same number of GMP blocks in four frames. This GMP block count serves as the $P_{m,server}$ parameter in the GMP algorithm.

Client Mode	Number of 257-bit Blocks in 1 GMP Block	Number of 257-bit Blocks in 4 Frames	Number of GMP blocks In 4 Frames
100G	1	10220	10220
200G	2	20440	10220
300G	3	30660	10220
400G	4	40880	10220

Table 4-1 – GMP Block Counts

4.4 Mapping of client traffic into ZR400

Figure 4-2 describes how data and stuffing are used in the ZR400 frame. For the 400G container, each GMP block is 4×257-bit blocks. Each GMP block containers either data or stuffing. The GMP mapping scheme operates over a period of four ZR400 frames. The number of stuffing blocks in a frame is defined by the Cm value that is stored in the ZR400 frame OH. A new Cm value is made available every four ZR400 frames.

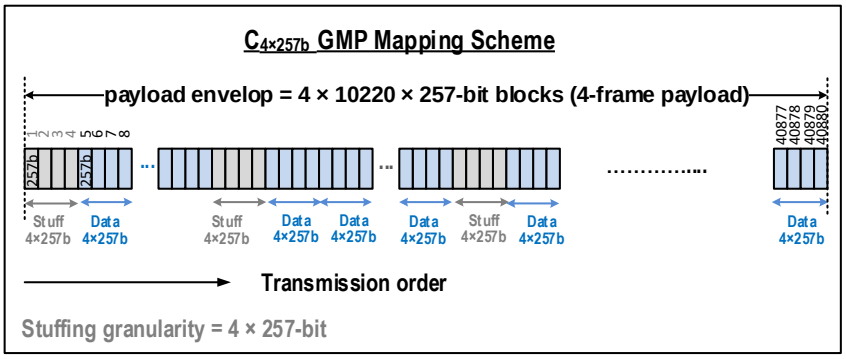


Figure 4-2 - Mapping of Client Traffic into ZR400

The number of 257-bit blocks in a GMP block is a function of the ZR400 container rate as defined in Figure 4-3.

The ZR400 GMP overhead for this mapping consists of:

- Three justification control (JC1, JC2, JC3) bytes carrying the value of GMP overhead Cm;
- Three justification control (JC4, JC5, JC6) bytes carrying the value of GMP overhead ∑ CnD.

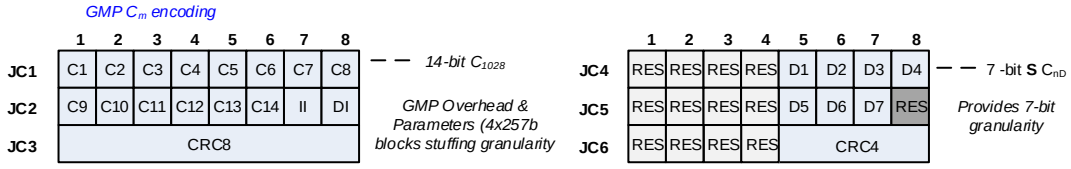


Figure 4-3 – Justification Control

The JC1, JC2 and JC3 bytes consist of a 14-bit Cm field (bits C1, C2, .., C14), a 1-bit Increment Indicator (II) field, a 1-bit Decrement Indicator (DI) field and an 8-bit CRC-8 field which contains an error check code over the JC1, JC2 and JC3 fields.

The JC4, JC5 and JC6 bytes consist of a 7-bit CnD field (bits D1, D2, .., D7), a 4-bit CRC-8 field which contains an error check code over the JC4, JC5 and JC6 fields.

The ZR400 payload consists of some number of GMP blocks (seeTable 4-2). Each GMP block consists of some number of 257-bits blocks (seeTable 4-1*)*.

The ZR400 signal is created from a locally generated clock which is independent of the client signal. The client signal is adapted to the locally generated ZR400 clock by means of a generic mapping procedure (GMP) as specified in G.709 Annex D. The generic mapping process generates the Cm(t) and CnD(t) information, once per four ZR400 frames, according to Annex D and encodes this information in the justification control overhead JC1/JC2/JC3 and JC4/JC5/JC6. The de-mapping process decodes Cm(t) and CnD(t) from JC1/JC2/JC3 and JC4/JC5/JC6 and interprets Cm(t) and CnD(t) according to Annex D. CRC-8 shall be used to protect against an error in JC1/JC2/JC3 and CRC4 protect against and error JC4/JC5/JC6 signals.

4.5 Generic Mapping Procedure Principles

Reference: G.709 Annex D.

The values of n, m, M, f_{client}, f_{server}, T_{server}, B_{server}, and $P_{m,server}$ for client mapping into the ZR400 are shown in Table 4-2.

Ref	GMP Parameter	Formula	Client Mapping			Units
			400GE to ZR400	200GE to ZR200	100GE to ZR100	
f_{client}	nominal client information bit rate		401,542,892,456.055	200,771,446,228.027	100,390,625,000.000	b/s
Δf_{client}	client bit rate tolerance		100	100	100	ppm
f_{server}	server nominal bit rate		402,489,753,309.729	201,244,876,654.865	100,622,438,327.432	b/s
Δf_{server}	server bit rate tolerance		20	20	20	ppm
T_{server}	period of the server multi-frame	B_{server} / f_{server}	26.154	26.154	26.154	µs
B_{server}	number of bits per server multi-frame		10,526,720	5,263,360	2,631,680	b
O_{server}	number of overhead bits per server multi-frame		20,560	10,280	5,140	b
P_{server}	number of payload bits per server multi-frame	B_{server} - O_{server}	10,506,160	5,253,080	2,626,540	b
$f_{p,server}$	nominal server payload bit rate	f_{server} x P_{server} / B_{server}	401,703,640,510.296	200,851,820,255.148	100,425,910,127.574	b/s
m	GMP data/stuff granularity		1,028	514	257	b
M	m and n ratio	m/n	128	128	128	
$P_{m,server}$	Max number of (m bits) in server payload area	P_{server}/m	10,220	10,220	10,220	1028b blocks
C_m	Number of client m-bit data entities per server multi-frame at nominal rates					
$C_{m,nom}$	Cm value at nominal client and server bit rates	$(f_{client} / f_{p,server}) \times P_{m,server}$	10215.910	10215.910	10216.409	
$C_{m,min}$	Cm at min client, max server rates	$C_{m,nom} \times (1 - \Delta f_{client}) / (1 + \Delta f_{server})$	10214.684	10214.684	10215.183	
$C_{m,max}$	Cm at max client, min server rates	$C_{m,nom} \times (1 + \Delta f_{client}) / (1 - \Delta f_{server})$	10217.136	10217.136	10217.635	
$C_{m,min}$	integer value of Cm,min	$\lfloor C_{,min} \rfloor$	10214	10214	10215	
$C_{m,max}$	rounded up value of Cm,max	$\lceil C_{m,max} \rceil$	10218	10218	10218	
n	GMP justification accuracy, n bit data entity		8.03125	4.01563	2.00781	b
$P_{n,server}$	Max number of (n bits) data entities in the server payload area	P_{server} / n	1,308,160	1,308,160	1,308,160	8.03125b blocks

Ref	GMP Parameter	Formula	Client Mapping			Units
			400GE to ZR400	200GE to ZR200	100GE to ZR100	
C_n	Number of client n-bit data entities per server multi-frame at nominal rates					
$C_{n,nom}$	Cn value at nominal client and server bit rates	$(f_{client} / f_{p,server}) \times P_{n,server}$	1,307,636.519	1,307,636.519	1,307,700.372	
$C_{n,min}$	Cn at min client, max server rates	$C_{n,nom} \times (1 - \Delta f_{client}) / (1 + \Delta f_{server})$	1,307,479.606	1,307,479.606	1,307,543.451	
$C_{n,max}$	Cn at max client, min server rates	$C_{n,nom} \times (1 + \Delta f_{client}) / (1 - \Delta f_{server})$	1,307,793.439	1,307,793.439	1,307,857.299	
C_{nD}	remainder of C_n and C_m		0.910305637	0.910305637	0.409153740	
C_{nD}	integer value of C_{nD}					
ΣC_{nD}	accumulated value of C_{nD}		127	127	127	

Table 4-2 – Client and ZRx GMP parameter values

Where,

- Nominal client information bit rates for 400GE and 200GE are nominal 400GBASE-R and 200GBASE-R rates after RS(544,514) FEC and AM removal. Nominal client information bit rate for 100GE clients with FEC is the nominal 100GBASE-R rate after RS(544,514) FEC removal. For 100GE clients without FEC, it is the nominal 100GBASE-R rate after transcoding from 64B66B to 256B257B blocks.
- Server is ZR400, ZR200 or ZR100 4-frame multi-frame (both payload and overhead), with f_{server} nominal bit rate, Δf_{server} bit rate tolerance and B_{server} number of bits per server 4-frame multi-frame.
- Server payload is ZR400, ZR200 or ZR100 4-frame multi-frame payload (before AM/PAD/OH insert), with $f_{p,server}$ nominal bit rate, Δf_{server} bit rate tolerance and P_{server} number of bits per server 4-frame multi-frame payload area.
- The maximum number_of_m [=1028] bit GMP data entities per 4-frame multi-frame payload is $P_{m,server}$ [=10220, or 5110, or 2555].
- For ZR400, ZR200 or ZR100, we use n = [m / 128] = [4×257-bit]/128 = 8.03125 UI that is used as a phase unit "n-bit equivalent" for C_n parameter. C_n indicates the number of "n-bit equivalent" of the xGBASE-R client per ZRx 4-frame multi-frame server payload. It can be used as a finer phase indicator to encode the client clock at the GMP mapper.
- So, $C_{n,\,nom} = 128 \times C_{m,\,nom}$; $C_{n,\,min} = 128 \times C_{m,\,min}$; $C_{n,\,max} = 128 \times C_{m,\,max}$
- $C_m = P_{m,server} \times$ [client_bit_rate / Server_Payload_bit_rate].
- C_m is an integer value indicating to every ZRx frame the number of m-bit client blocks carried [m = 4×257b = 1028b] in this ZRx 4-frame server multi-frame payload = int($P_{m,server}$×[client_bit_rate/Server_Payload_bit_rate]).
- $C_m \leq P_{m,server}$ and is a value varying between $C_{m,min}$ and $C_{m,max}$ for the given client and payload type, due to client and payload bit rate tolerance range (+/- 100 ppm and +/-20 ppm).

4.6 Stuffing Locations

Table 4-3 shows the location of the "stuff" GMP blocks for a few specific Cm values.

Cm	Stuff Locations (index values of 4×257b locations in 4-frame multi-frame)
10220	N/A
10219	1
10218	1, 5111
10217	1, 3407, 6814
10216	1, 2556, 5111, 7666
10215	1, 2045, 4089, 6133, 8177
10216	1, 1704, 3407, 5111, 6814, 8517

Table 4-3 – GMP STUFF Locations of ZR400

5 Multiplexing

Multiplexing of 100G and 200G clients into the ZR400 frame, illustrated in Figure 5-1, is performed using simple time division multiplexing of the 257-bit blocks in the ZR payload. A ZR400 frame has four sets of overhead (OH) available in the first row to support multiplexing of GMP for up to four clients.

There are 10220 257-bit blocks in a ZR400 frame. This number is divisible by both 4 and 2. Row 1 has 20 blocks, while all other rows have 40 blocks. The ZR400 stuffing location uses some number of consecutive 257-bit blocks based upon ZR400 rate as shown in Table 4-1. The ZR400 frame has 4 unique OH chunks of 40 bytes. The GMP six justification control bytes are distributed inside the OH using four consecutive frames. There are two GMP values processed during the 8-frame ZR400 multi-frame.

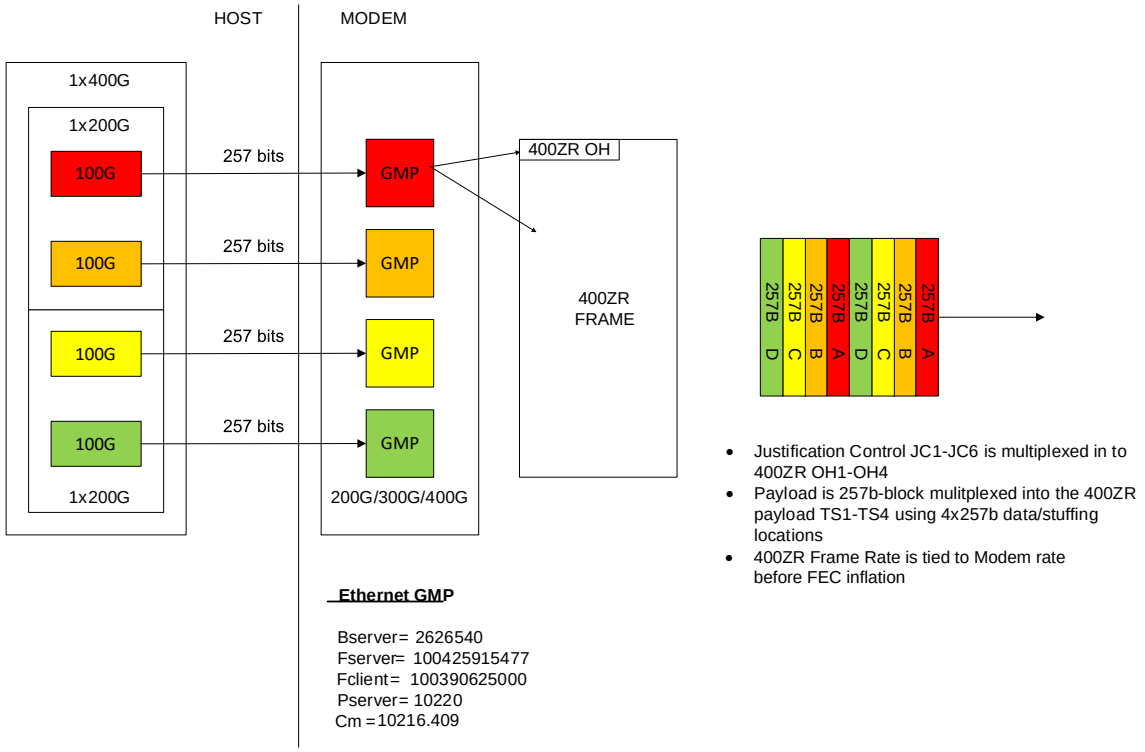


Figure 5-1 – 100G, and 200G Multiplexing in ZR400 Frame

5.1 ZR400 Frame Structure

The ZR400 frame structure is 10280b × 256 rows with 1920b columns of AM, 1920b columns of PAD, and 1280b of OH and 20-bits of additional pad located in row 1 bits 5121 through 5140. The additional pad is to align the payload area on a 257b boundary. Parity is added by the OFEC block and interleaver stages downstream of the ZR400 frame structure.

The ZR400 frame structure is shown in Figure 5-2.

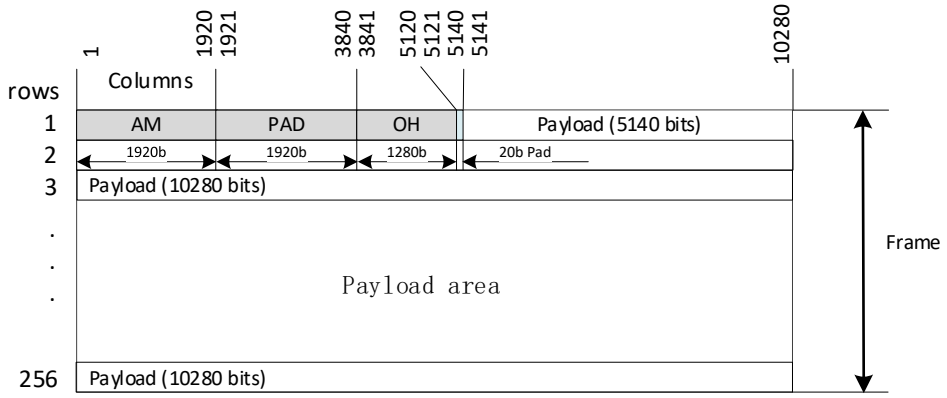


Figure 5-2: ZR400- frame structure

- There are 10220 257-bit blocks in a ZR400 frame. This number is divisible by both 4 and 2.

- Row 1 has 20-blocks, all other rows have 40 blocks.
- The ZR400 stuffing location uses 4 consecutive 257-bit blocks.
- The ZR400 frame has 4 unique OH chunks of 40 bytes. The GMP is distributed across 4 consecutive frames in the 40-byte OH. There are 2 GMP values processed during the 8 frame ZR400 multi-frame.
- Multiplexing scheme defines 4×100G and 2×200G.
- Cm/Cnd distributed across OH in 4 frames.
- Cm/Cnd value extracted in current 4 frame set used in next 4 frame set.

5.1.1 400G Container Multiplexing

This section describes how 100G, and 200G, clients are multiplexed in a ZR400 container.

For multiplexed signals, the AM, PAD, and OH from four frame/multi-frame aligned ZR100 frames or from two frame/multi-frame aligned ZR200 frames and additional pad are 10-bit interleaved. The payload area is 257b interleaved.

This process is shown in Figure 5-3.

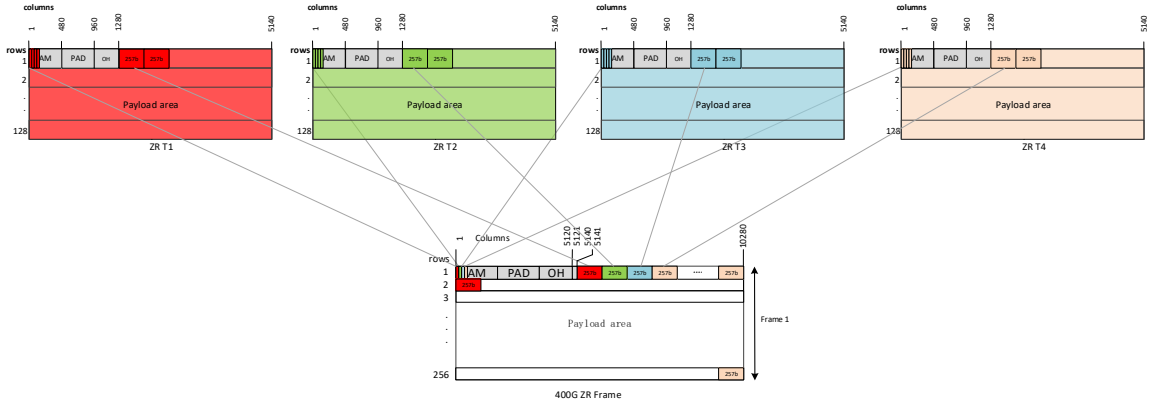


Figure 5-3: 4 Interleaved ZR100 frame to ZR400 frame structure

- 4 100G tributaries numbered T1, T2, T3, T4.
- 10220 257-block locations are numbered 1 through 10220, ordered left to right, top to bottom in ZR400 frame view.
- Each tributary assigned 2555 257-bit blocks.
- T1 consumes locations 1, 5, 9…,10217
- T2 consumes locations 2, 6, 10…,10218
- T3 consumes locations 3, 7, 11…,10219
- T4 consumes locations 4, 8, 12…,10220
- Simple round-robin ordering.
- 4 Unique 40-byte OH sections in each ZR400 frame, ordered left to right, in ZR400 frame view, numbered OH1, OH2, OH3, OH4
- 4×257-bit stuffing locations.
- Each 4×257-bit stuffing block divided into 4 stuffing locations numbered S1 through S4, ordered left to right in ZR400 frame.
- Each tributary assigned 1 257-bit block of stuffing.
- T1 uses S1

- T2 uses S2
- T3 uses S3
- T4 uses S4
- Stuffing location defined by CM value of each OH.
- Every 4×257-bit stuffing location will have mix of data and stuff when multiplexing in play.
- 4 Unique OH numbered OH1, OH2, OH3, OH4.
- T1 uses OH1
- T2 uses OH2
- T3 uses OH3
- T4 uses OH4

5.1.2 1×400G Data Multiplexing

- 1 400G client numbered CL1.
- 400G client assigned all four tributaries.
- The GMP for the client is stored in the assigned overhead.

5.1.3 2×200G Data Multiplexing

- 2 200G clients numbered CL1, CL2.
- Each client assigned two tributaries and two corresponding overhead.
- Tributaries assigned to client need not be consecutive, but data is ordered with first data in time assigned to lower ordinal tributary.
- The GMP for the client is stored in the overhead with the lowest ordinal number.

5.1.4 4×100G Data Multiplexing

- 4 100G clients numbered CL1, CL2, CL3, CL4.
- Each client assigned one tributary and one corresponding overhead.
- The GMP for the client is stored in the overhead with the lowest ordinal number (OH1).
- Alignment markers are inserted in the 100G data stream to transparently pass the BIP3/BIP7 values across transport layer.
- The alignment marker follows the rules defined in 802.3 Clause 91 and G.709 Annex E with one exception:
    - When looking at 802.3 Clause 91.5.2 Figure 91-4; the values in amp_tx_0,1,2,3,16,17,18,19 are replaced with the unique values for those 8 logical lanes, as defined by Clause 82.2.7 Table 82-2.
- The alignment markers consume 5 consecutive 257-bit blocks using the intervals defined in Clause 91.
- The alignment markers are constructed using 128 10-bit symbols followed by the 5-bit pad as defined in Clause 91. The 128 10-bit symbols plus 5-bit pad combine to form 5 257-bit blocks.
- The order of the 10-bit symbols can be referenced using 802.3 Clause 91 Figure 91-4 with the symbols extracted top-to-bottom, left-to-right from the box in this figure with the 5-bit pad following at the end.

5.2 ZR300 Frame Structure

The ZR300 frame structure is 10280b × 192 rows with 1440b columns of AM, 1440b columns of PAD, and 960b of OH and 15-bits of additional pad located in row 1 bits 3841

through 3855. The additional pad is to align the payload area on a 257b boundary. Parity is added by the OFEC block and interleaver stages downstream of the ZR300 frame structure.

The ZR300 frame structure is shown in Figure 5-4.

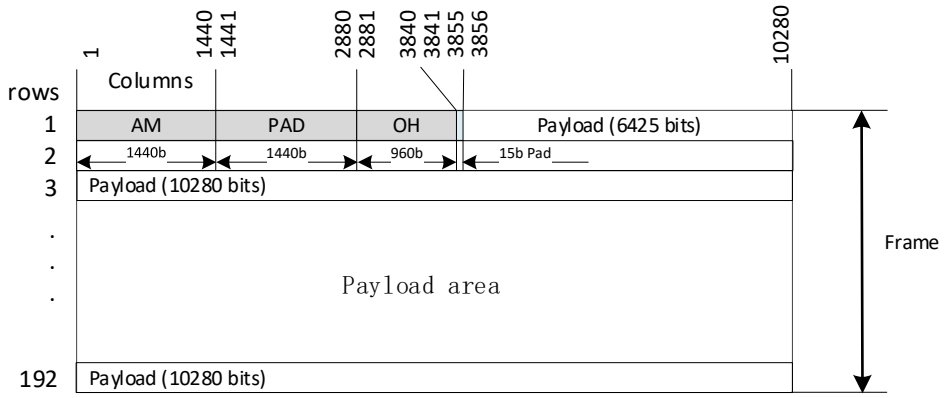


Figure 5-4: ZR300 frame structure

5.2.1 300G Container Multiplexing

This section describes how 100G and 300G clients are multiplexed in a ZR300 container.

For multiplexed signals, the AM, PAD, and OH, from three frame/multi-frame aligned ZR100 frames and additional pad are 10b interleaved. The payload area is 257b interleaved.

This interleaving process is shown in Figure 5-5.

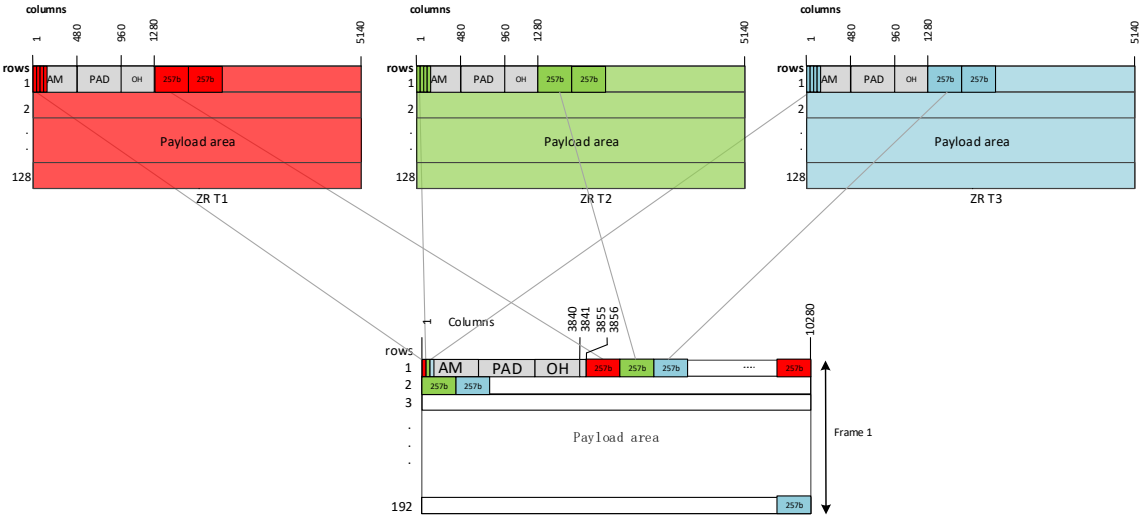


Figure 5-5: Three interleaved ZR100 frames to ZR300 frame structure

- 3 100G tributaries numbered T1, T2, T3.
- 7665 257-block locations are numbered 1 through 7665, ordered left to right, top to bottom in ZR400 frame view.
- Each tributary assigned 2555 257-bit blocks.
- T1 consumes locations 1, 4, 7…,7663

- T2 consumes locations 2, 5, 8…,7664
- T3 consumes locations 3, 6, 9…,7665
- Simple round-robin ordering.
- 3 Unique 40-byte OH sections in each ZR300 frame, ordered left to right, in ZR300 frame view, numbered OH1, OH2, OH3.
- 3×257-bit stuffing locations.
- Each 3×257-bit stuffing block divided into 3 stuffing locations numbered S1 through S3, ordered left to right in ZR300 frame.
- Each tributary assigned 1 257-bit block of stuffing.
- T1 uses S1
- T2 uses S2
- T3 uses S3
- Stuffing location defined by CM value of each OH.
- Every 3×257-bit Stuffing location will have mix of data and stuff when multiplexing in play.
- 3 Unique OH numbered OH1, OH2, OH3.
- T1 uses OH1
- T2 uses OH2
- T3 uses OH3

5.2.2 3×100G Data Multiplexing

- 3 100G clients numbered CL1, CL2, CL3.
- Each client assigned one tributary and one corresponding overhead.
- The GMP for the client is stored in the assigned overhead.
- Alignment markers are inserted in the 100G data stream to transparently pass the BIP3/BIP7 values across transport layer.
- The alignment marker follows the rules defined in 802.3 Clause 91 and G.709 Annex E with one exception:
    - When looking at 802.3 Clause 91.5.2 Figure 91-4; the values in amp_tx_0,1,2,3,16,17,18,19 are replaced with the unique values for those 8 logical lanes, as defined by Clause 82.2.7 Table 82-2.
- The alignment markers consume 5 consecutive 257-bit blocks using the intervals defined in Clause 91.
- The alignment markers are constructed using 128 10-bit symbols followed by the 5-bit pad as defined in Clause 91. The 128 10-bit symbols plus 5-bit pad combine to form 5 257-bit blocks.
- The order of the 10-bit symbols can be referenced using 802.3 Clause 91 Figure 91-4 with the symbols extracted top-to-bottom, left-to-right from the box in this figure with the 5-bit pad following at the end.

5.3 ZR200 Frame Structure

The ZR200 frame structure is a block format of 10280-bit columns × 128 rows with 960b columns of AM, 960b columns of PAD, and 640b of OH and 10-bits of additional pad located in row 1 bits 1921 through 2560. The additional pad is to align the payload area on a 257b boundary. Parity is added by the OFEC block and interleaver stages downstream of the ZR200 frame structure.

The ZR200 frame structure is shown in Figure 5-6.

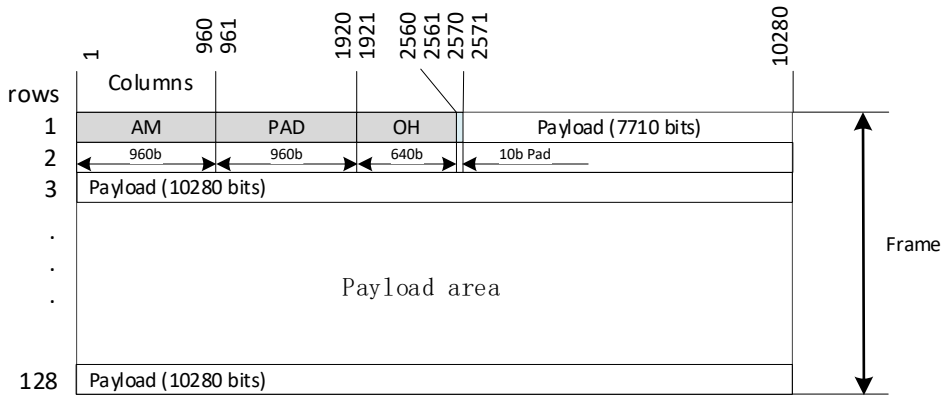


Figure 5-6: ZR200 frame structure

5.3.1 200G Container Multiplexing

This section describes how 100G and 200G clients are multiplexed in a ZR200 container.

For multiplexed signals, the AM, PAD, and OH, from two frame/multi-frame aligned ZR100 frames and additional pad are 10b interleaved. The payload area is 257b interleaved.

The interleaving process is shown in Figure 5-7.

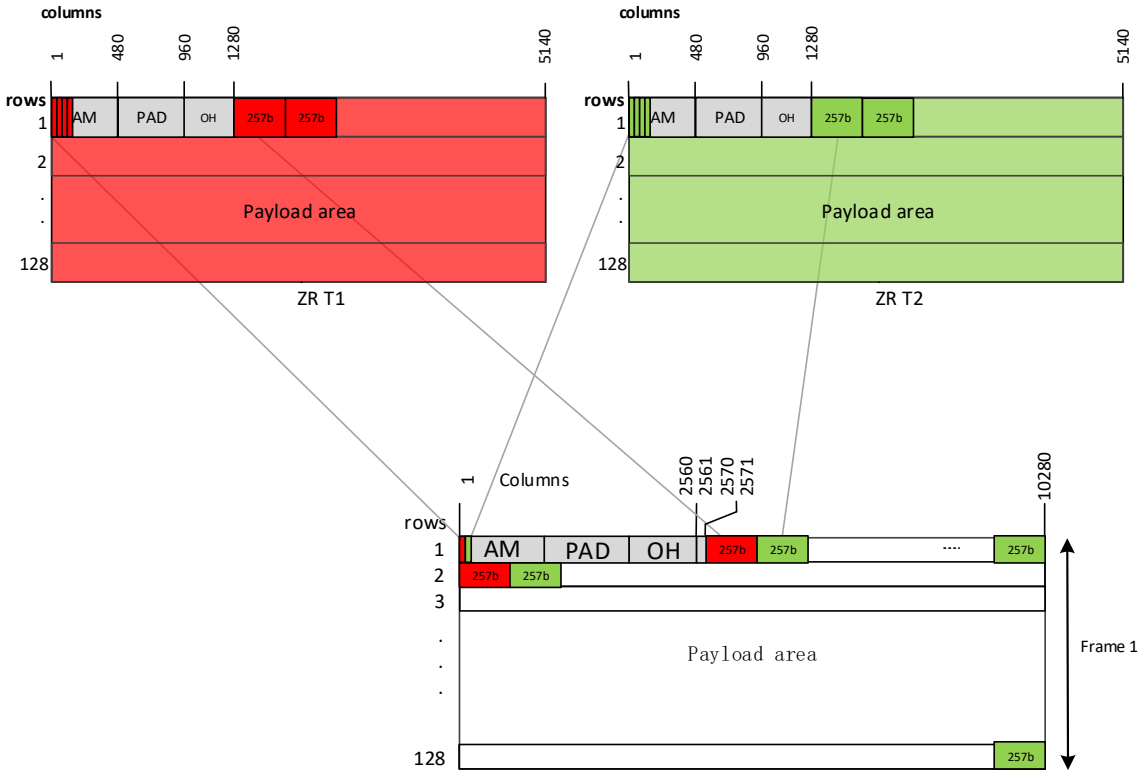


Figure 5-7: Two interleaved ZR100 frames to a ZR200 frame structure

- 2 100G tributaries numbered T1, T2.
- 5110 257-block locations are numbered 1 through 5110, ordered left to right, top to bottom in ZR400 frame view.
- Each tributary assigned 2555 257-bit blocks.

- T1 consumes locations 1, 3, 5, …, 5109
- T2 consumes locations 2, 4, 6, …, 5110
- Simple round-robin ordering.
- 2 Unique 40-byte OH sections in each ZR400 frame, ordered left to right, in ZR400 frame view, numbered OH1, OH2.
- 2×257-bit stuffing locations.
- Each 2×257-bit stuffing block divided into 2 stuffing locations numbered S1 through S2, ordered left to right in ZR400 frame.
- Each tributary assigned 1 257-bit block of stuffing.
- T1 uses S1
- T2 uses S2
- Stuffing location defined by CM value of each OH.
- Every 2×257-bit Stuffing location will have mix of data and stuff when multiplexing in play.
- 2 Unique OH numbered OH1, OH2.
- T1 uses OH1
- T2 uses OH2

5.3.2 1×200G Data Multiplexing

- 1 200G client numbered CL1.
- 200G client assigned all two tributaries.
- The GMP for the client is stored in the assigned overhead.

5.3.3 2×100G Data Multiplexing

- 2 100G clients numbered CL1, CL2.
- Each client assigned one tributary and one corresponding overhead.
- The GMP for the client is stored in the overhead with the lowest ordinal number (OH1).
- The alignment marker follows the rules defined in 802.3 Clause 91 and G.709 Annex E with one exception:
    - When looking at 802.3 Clause 91.5.2 Figure 91-4; the values in amp_tx_0,1,2,3,16,17,18,19 are replaced with the unique values for those 8 logical lanes, as defined by Clause 82.2.7 Table 82-2.
- The alignment markers consume 5 consecutive 257-bit blocks using the intervals defined in Clause 91.
- The alignment markers are constructed using 128 10-bit symbols followed by the 5-bit pad as defined in Clause 91. The 128 10-bit symbols plus 5-bit pad combine to form 5 257-bit blocks.
- The order of the 10-bit symbols can be referenced using 802.3 Clause 91 Figure 91-4 with the symbols extracted top-to-bottom, left-to-right from the box in this figure with the 5-bit pad following at the end.

5.4 ZR100 frame structure

The ZR100 frame structure is like the FlexO-1 frame structure defined in G.709.1 (G.709.1/Y.1331(18) _F8-1) copied as Figure 5-8 for reference. FlexO is a block format of 5140-bit columns × 128 rows. The ZR100 frame structure in Figure 5-9 is also a block format of 5140-bit columns × 128 rows, however, it includes a 5-bit pad located in row 1 bits 1281 through 1285. The additional pad is to align the payload area on a 257b boundary.

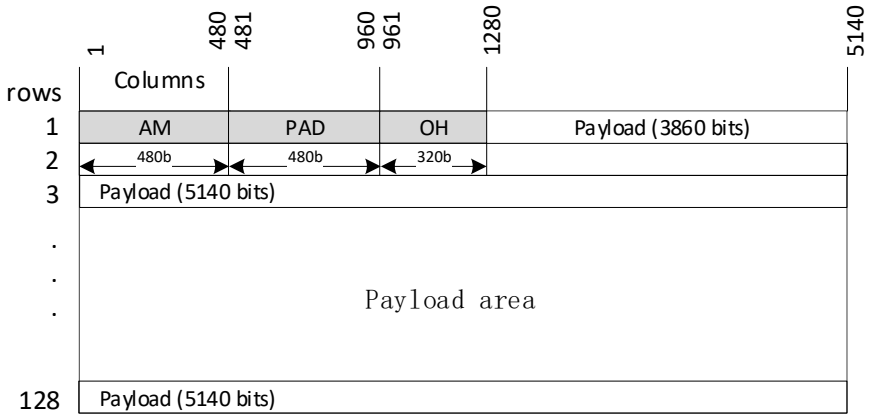


Figure 5-8: FlexO frame structure (reference)

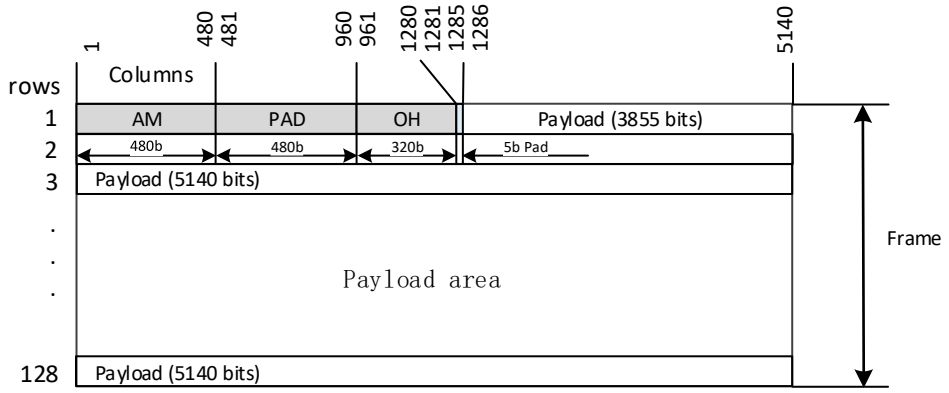


Figure 5-9: ZR100 frame structure

5.4.1 100G Container Multiplexing

This section describes how 100G is multiplexed in a 100G ZR container.

- 1 100G tributaries numbered T1.
- 2555 257-bit block locations are numbered 1 through 2555, ordered left to right, top to bottom in ZR400 frame view.
- Each tributary assigned 2555 257-bit blocks.
- T1 consumes locations 1, 2, 3…,2555
- 1 Unique 40 byte OH sections in each ZR400 frame, ordered left to right, in ZR400 frame view, numbered OH1.
- 1×257-bit stuffing locations numbered S1.
- Each tributary assigned 1 257-bit block of stuffing.
- T1 uses S1
- Stuffing location defined by CM value of each OH.
- 1 Unique OH numbered OH1.
- T1 uses OH1

5.4.2 1x100G Data Multiplexing

- 1 100G client numbered CL1.

- 1 100G tributaries numbered T1.
- 1 Unique OH numbered OH1.
- CL1 assigned tributary T1 and overhead OH1.
- The GMP for the client is stored in the overhead with the lowest ordinal number (OH1).
- The alignment marker follows the rules defined in 802.3 Clause 91 and G.709 Annex E with one exception:
    - When looking at 802.3 Clause 91.5.2 Figure 91-4; the values in amp_tx_0,1,2,3,16,17,18,19 are replaced with the unique values for those 8 logical lanes, as defined by Clause 82.2.7 Table 82-2.
- The alignment markers consume 5 consecutive 257-bit blocks using the intervals defined in Clause 91.
- The alignment markers are constructed using 128 10-bit symbols followed by the 5-bit pad as defined in Clause 91. The 128 10-bit symbols plus 5-bit pad combine to form 5 257-bit blocks.
- The order of the 10-bit symbols can be referenced using 802.3 Clause 91 Figure 91-4 with the symbols extracted top-to-bottom, left-to-right from the box in this figure with the 5-bit pad following at the end

6 ZRx adaptation to OFEC

The ZRx frame structure is adapted to the OFEC Coder block by adding padding after every n × 10280-bit rows. The data stream is then scrambled and passed to the OFEC encoder. Table 6-1 shows the relationships between the OFEC-x Coder Payload and the ZRx frame structure. The ZRx-OFEC is aligned and synchronized to the DSP frame, therefore the number of PAD bits, OFEC block and payload bits per DSP frame is modulation dependent.

	ZRx Rows	PAD (bits)	OFEC-x coder payload (bits)	OFEC Blocks	ZRx (bits)	Modulation Format
ZR400	116 rows	992	1,193,472	168	1,376,256	16QAM
ZR300	87 rows	744	895,104	126	1,032,192	8QAM
ZR200	58 rows	496	596,736	84	688,128	QPSK
ZR100	116 rows	496	596,736	84	688,128	QPSK

Table 6-1: OFEC adaptation rates

The digital formatting and processing done by the DSP to adapt the FlexO-x to the OFEC Coder is shown in Figure 6-1.

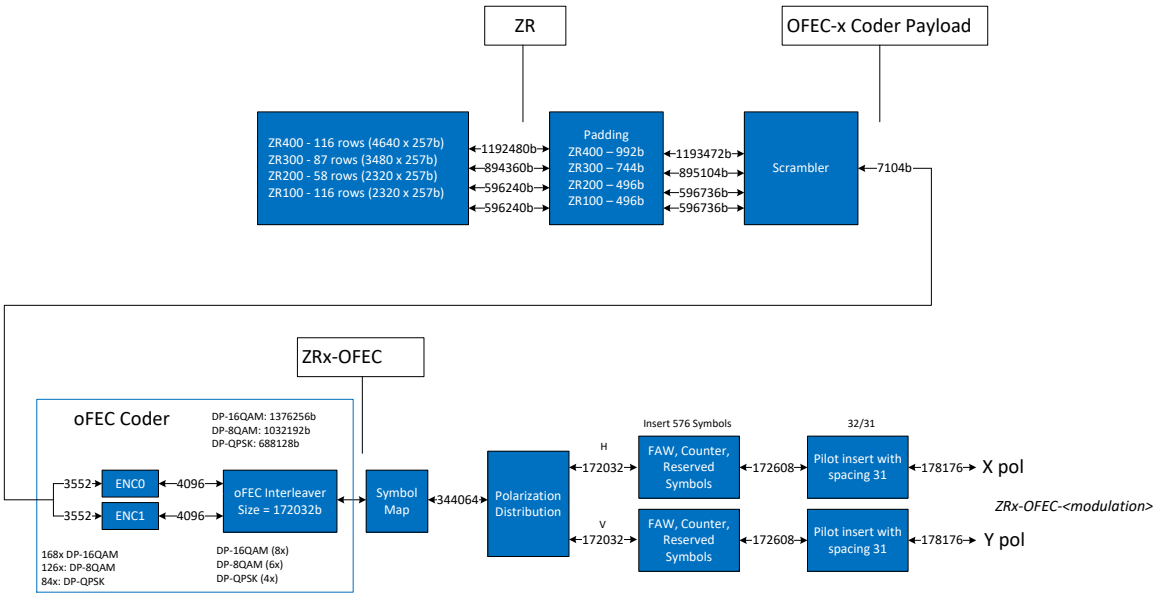


Figure 6-1: Digital processes of ZR-x to ZRx-OFEC adaptation.

6.1 Padding Insertion/Removal

The OFEC block processing is aligned and synchronized to the DSP super-frame (See Section 9.1). Pad bits are appended to the ZRx framed data to enable this alignment. The PAD is removed after the decoder on the receive interface. The PAD is an all-zero field that gets scrambled prior to encoding and removed after decoding and descrambling.

6.2 ZR400 adaptation to ZR400-OFEC-16QAM

For ZR400 adaptation to a ZR400-OFEC-16QAM line interface, 116 rows of ZR400 information (1,192,480 bits) plus 992 bits of pad (1,193,472 bits total) are scrambled and then bitwise demultiplexed to two OFEC encoders, each of which operate on input blocks

of 3,552 bits and produce output blocks of 4096 bits. To process the 1,193,472 bits each encoder operates on 168 input blocks of 7104 bits.

Figure 6-2 shows the adaptation of the ZR400 frame structure to the OFEC input block structure.

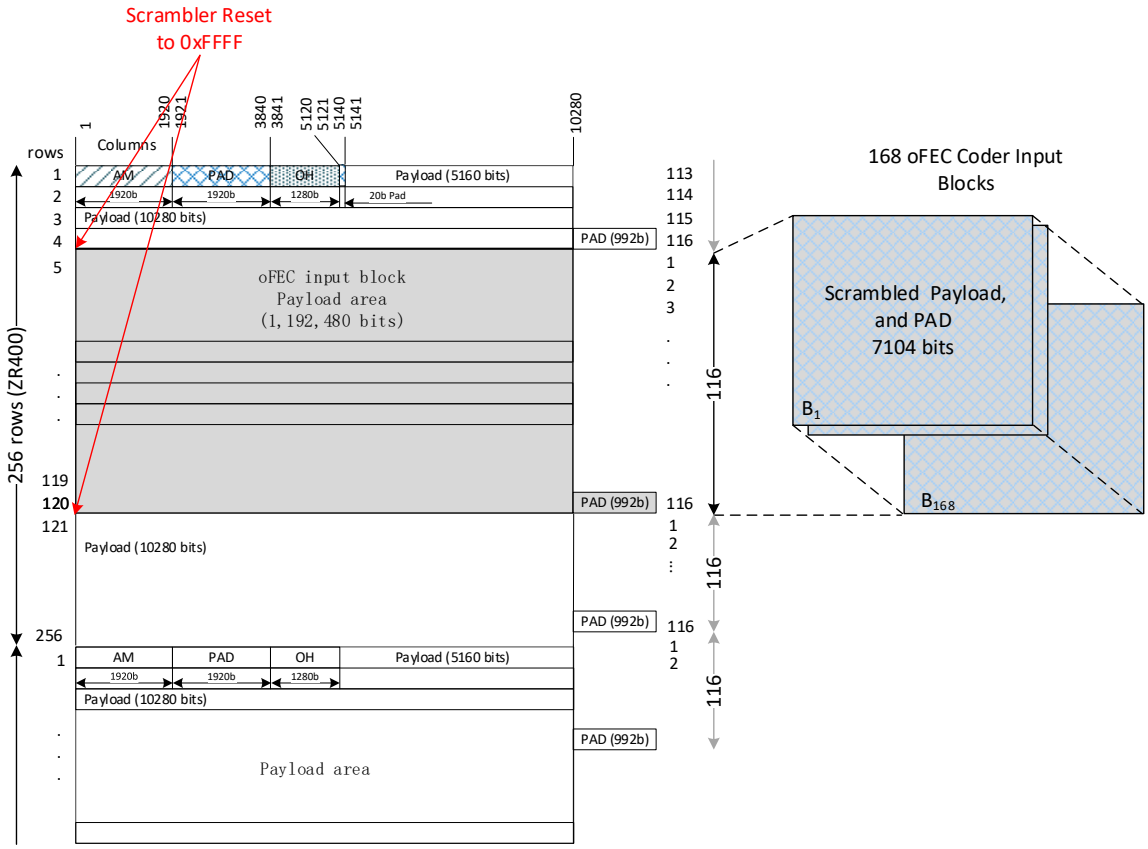


Figure 6-2: ZR400 adaptation to a ZR400-OFEC-16QAM line interface

6.3 ZR300 adaptation to ZR300-OFEC-8QAM

For ZR300 adaptation to an ZR300-OFEC-8QAM line interface 87 rows of ZR300 information (894,360 bits) plus 744 bits of pad (895,104 bits total) are scrambled and then bitwise demultiplexed to two OFEC encoders, each of which operate on input blocks of 3552 bits and produce output blocks of 4,096 bits. To process the 895,104 bits each encoder operates on 126 input blocks of 7104 bits.

Figure 6-3 shows the adaptation of the ZR300 frame structure to the OFEC input block structure.

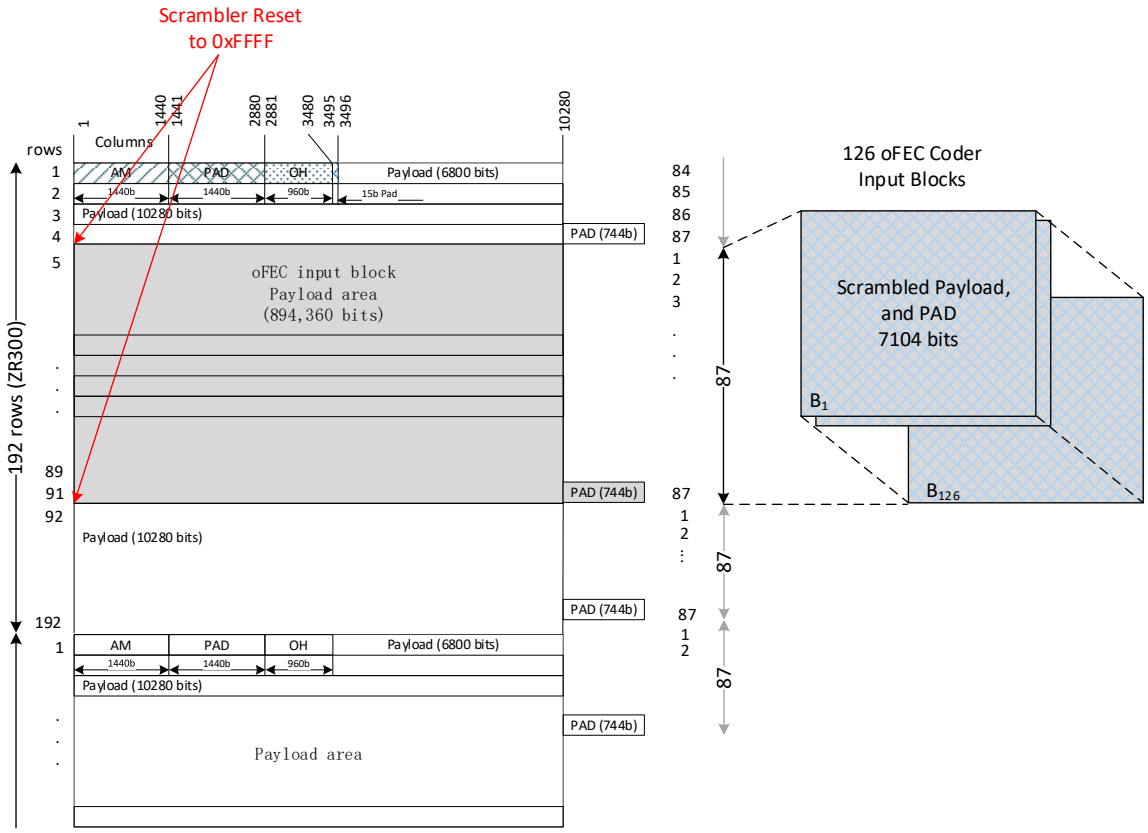


Figure 6-3: ZR300 adaptation to a ZR300-OFEC-8QAM line interface

6.4 ZR200 adaptation to ZR200-OFEC-QPSK

For ZR200 adaptation to an ZR200-OFEC-QPSK line interface 58 rows of ZR200 information (596,240 bits) plus 496 bits of pad (596,736 bits total) are scrambled and then bitwise demultiplexed to two OFEC encoders, each of which operate on input blocks of 3,552 bits and produce output blocks of 4,096 bits. To process the 596,736 bits each encoder operates on 84 input blocks of 7104 bits.

Figure 6-3 shows the adaptation of the ZR200 frame structure to the OFEC input block structure.

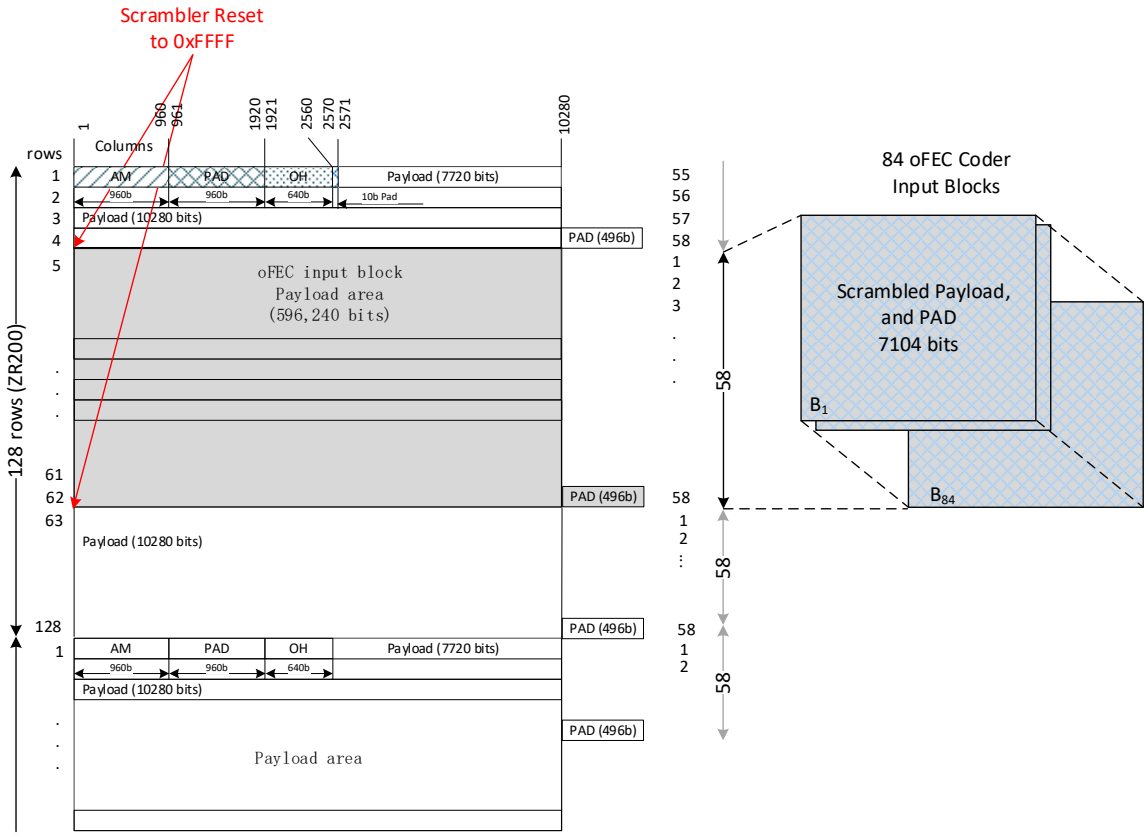


Figure 6-4: ZR200 adaptation to a ZR200-OFEC-QPSK line interface

6.5 ZR100 adaptation to OFEC input blocks

For ZR100 116 rows of information (596,240 bits) plus 496 bits of pad (596,736 bits total) are scrambled and then bitwise demultiplexed to two OFEC encoders, each of which operate on input blocks of 3,552 bits and produce output blocks of 4,096 bits. To process the 596,736 bits each encoder operates on 84 input blocks of 7104 bits.

Figure 6-3 shows the adaptation of the ZR100 frame structure to the OFEC input block structure and then to the encoder input block sequence.

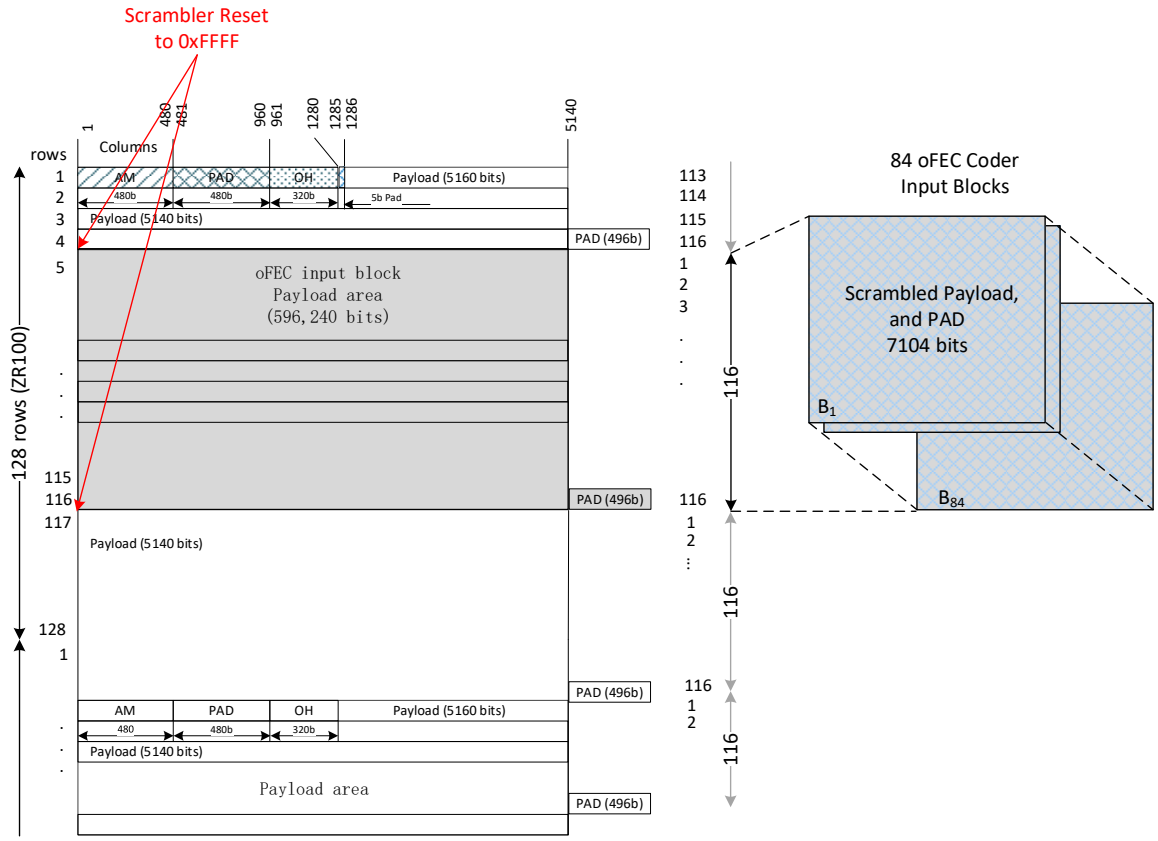


Figure 6-5: ZR100 adaptation to a ZR100-OFEC-QPSK line interface

6.6 Frame Synchronous Scrambling

The scrambler/descrambler is located before OFEC encoder on transmit, and after the OFEC decoder on receive. The operation of the scrambler shall be functionally equivalent to that of a frame-synchronous additive scrambler of sequence 65535 and the generating polynomial shall be:

$$x^{16} + x^{12} + x^{3} + x + 1$$

The scrambler/descrambler resets to 0xFFFF at the start of each new OFEC input block structure. The scrambler runs continuously over the entire OFEC input block. Figure 6-6 shows a functional diagram of the frame synchronous scrambler.

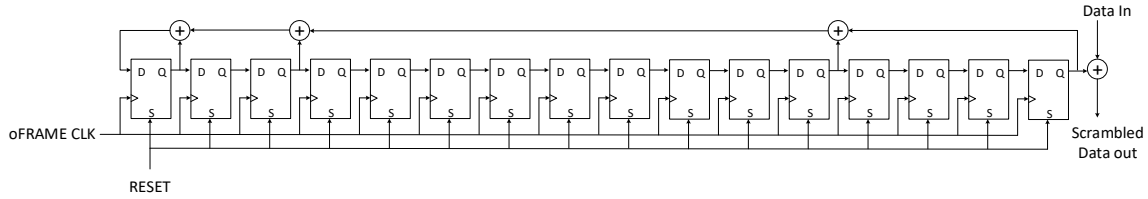


Figure 6-6: Frame synchronous scrambler

7 Open Forward Error Correction (OFEC)

NOTE: This section of the document uses zero-based indexing for mathematical formula convenience.

The OFEC encoding block shown in Figure 7-1 consists of two FEC encoders/decoders (ENC0 and ENC1) operating in parallel. 7,104 bits are bit de-interleaved/interleaved to/from each encoder/decoder. The encoder expansion ratio is 4096/3552.

The OFEC encoder and OFEC interleaver datapath is shown in Figure 7-1. The 7104 bits from the scrambler are bit demultiplexed into two parallel 3552/4096 encoder engines. Even numbered bits (0 based) go to encoder 0 (ENC0), and odd numbered bits to encoder 1 (ENC1).

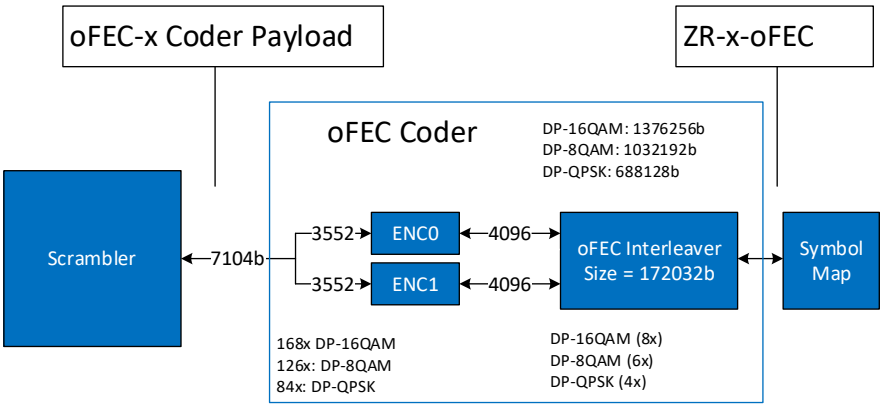


Figure 7-1: OFEC block encoder and OFEC Interleaver

7.1 OFEC encoding codec

Note: *The section below describes a single instance of the OFEC encoder engine, i.e. one of ENC0 or ENC1 in Figure 7-1.*

For the OpenZR+ applications two encoding engines operate in parallel, with each engine producing an OFEC codeword. A codeword in OFEC is a semi-infinite set of bits organized in a matrix with semi-infinite number of rows and N columns (N = 128).

It has the property that each bit is part of two "constituent component codewords," in which each constituent component codeword is a binary vector x of length 2N satisfying the parity check constraint xH = 0, where H is a (2N, 2N – k) binary parity check matrix, with 2N > k > N. Here k = 239, and each constituent component codeword has (2N – k) = 17 parity bits. The fraction of bits that are parity bits is 17/128, the rate of the code is 111/128 = 0.867, and the overhead is 17/111 = 15.3%.

Specifically, in OFEC, H is a parity check matrix of an extended BCH (256, 239) code. This BCH code has a minimum Hamming distance of 6. OFEC uses a BCH textbook encoding with a parity check matrix H that is specified below.

The constituent component codewords are ordered as explained below to allow high speed parallel encoding and decoding. To define what bits are part of a given constituent component codeword the following structure is used:

- The infinite matrix of bits is partitioned in square blocks of B × B bits (B = 16), arranged in rows and columns as shown in Figure 7-2. There are N/B blocks per row (N/B = 8), and each square block is identified by a square block row number, R, and a square block column number, C, where C= 0, 1, … , N/B–1, appearing respectively on the left hand side and at the top of the figure.
- Each bit inside a square block is identified by its row number, r, where r = 0, 1, …, B – 1, and column number, c, where c = 0, 1, …, B – 1, where bit 0, 0 is at the upper left corner of a block. Overall, each bit in the infinite matrix is identified by a quadruple {R, C, r, c}.
- The number of guard-block rows needs to be even with a value 2G, (e.g. G = 2, or 2G = 4 rows, in Figure 7-2)

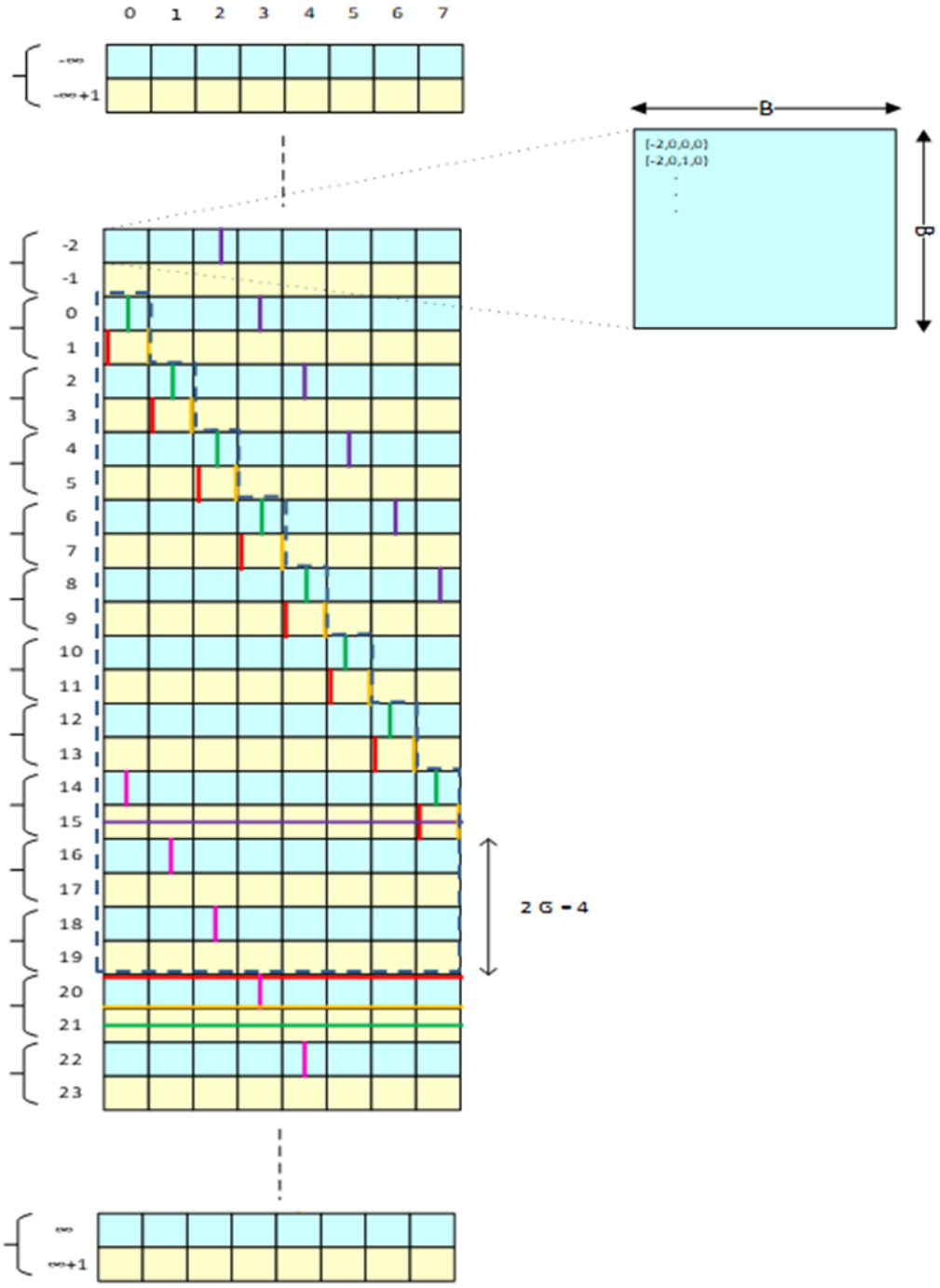


Figure 7-2: Structure of an openFEC Coder

A row of bits is identified by (R, r), with a square block row number R and a bit row number r within that block, where r = 0, 1, …, B – 1. A constituent component codeword can be identified by the number of the row that contains all bits of the 2nd half of the codeword. The kth bit (k = 0, 1, …, 2N – 1) of constituent component codeword (R, r) is the bit identified with the quadruple:

- If k < N: $\{(R \wedge 1) - 2G - 2\ N/B + 2\ [k/B], [k/B], (k\ \%\ B) \wedge r, r\}$ (1)
- If k ≥ N: $\{R, [(k - N)/B], r, (k\ \%\ B) \wedge r\}$ (2)

where,

[.] denotes the floor operator,

(a % b) denotes the value of a modulo b, and

(a ^ b) represents the number with a binary representation equal to the bitwise "exclusive or" of the binary representations of the numbers a and b.

These formulas are illustrated in Figure 7-2. The union of line segments (both vertical and horizontal) of a given color shows the bits forming a constituent component codeword but the ordering in the segments is not the ordering in the codeword.

For example, consider the constituent component codeword (20, 0). The position of its bits in the semi-infinite matrix are indicated by the red line segments. Bits 0 to 15 are in column 0 of block (1, 0), bits 16 to 31 in column 0 of block (3, 1), …, and bits 112 to 127 in column 0 of block (15, 7). The bit indices go up as one descends in the columns.

Bits 128 to 255 are in row 0 of blocks (20, 0) to (20, 7), and their indices go up moving to the right within a row.

Bits 0 to 127 are referred to as the "front" of a constituent component codeword, and bits 128 to 255 as the "back."

Note that each bit in the OFEC encoder belongs to the front of a constituent component codeword and to the back of another one. Also, if the back of a constituent component codeword is in an odd-numbered row of square blocks (yellow background), then its front is an even-numbered row of square blocks (blue background), and conversely.

The square blocks located below the "front bits" and above the "back bits" of a given constituent component codeword are so called guard blocks, relative to the constituent component codeword of interest.

Continuing the example, the bits of constituent component codeword (20, 15), identified by the orange line segments, are in the same blocks as the segments of constituent component codeword (20, 0). However, because "r" is 15 instead of 0 as in the previous example, the expressions "^ r" in formulas (1) and (2) become significant, and the bits are taken in reverse order in each block. For example, bits 0 to 15 in the front of codeword (20, 15) are bits 15 to 0 in column 15 of block (1, 0).

Note: The OFEC code is a block-convolutional code, and its performance is characterized by its "error events." Without the "^ r" permutation, there are about 625,000 possible error events of weight 36 that can start at every decoding of a constituent component codeword. For comparison, a Product Code based on the same constituent component codeword has more than 3.3e13 codewords of weight 36. The presence of the "^ r" permutation can be observed to eliminate error events of weight 36. Consequently, the minimum Hamming distance of the OFEC code is at least 42.

7.2 Encoding

Encoding is done sequentially, in order of increasing row index. At the time when a constituent component codeword (R, r) is being encoded, all constituent component codewords (R', r') with R' < R – 2G must already be encoded.

To encode a constituent component codeword (R, r), form a vector *x* of length 2N where the front N bits are read from previously encoded bits in the infinite matrix according to formula (1) above. In the back, the first k – N (i.e., 111) bits are fresh information bits. The last 2N – k (i.e., 17) back bits are parity bits that can be calculated to satisfy *x*H = 0. After encoding, the N back bits are placed at their positions in the infinite matrix according to formula (2) above, and bits in those positions are output to an interleaver.

Considering Figure 7-2, we see that G is large enough to allow the parallel encoding of 2 B (G + 1) = 96 constituent component codewords, assuming the pipeline delay is small. This number is considerably reduced when the pipeline delay increases, which is typically the case in the decoder.

One can also see that at most N/B (N/B + 2 G + 1) = 104 square blocks need to be kept in the encoder memory (excluding the current input). The square blocks that must be kept in memory to encode block rows 20 and 21 are surrounded by the dashed line in Figure 7-2.

A large G allows for longer pipeline delays in the encoding and decoding operations and allows for more parallel execution in the encoder and decoder, at the expense of increased memory.

7.3 Encoder interface

The encoder input consists of rectangular blocks of size (2B) × (2N – k) = 32 × 111 bits. The encoder input blocks are numbered 0, 1, 2, …. The input bits into the encoder are sequenced. The i^{th} input bit is placed in the encoder input block [i / (32 × 111)] at the position indicated by the value i % (32 × 111) in Figure 7-3. Note that an encoder input block is divided in 16×16-bit blocks, except along the right edge where their size is 16×15.

Bit k = 0, 1, 2… of row p in encoder input block P is placed in position N + k of constituent component codeword (2 P + [p/B], p % B).

0 1 … 15 16 17 … 31 32… . . . . 240 .. . 255	512… . . . . . . … 767	1024 … . . . . . . … 1279	1536 … . . . . . . … 1791	2048 … . . . . . . … 2303	2560 … . . . . . . … 2815	3072 3073 … 3086 3087 … 3101 3102 … 3599 . . . . 3297 … 3311	
256… 271 272 . . . . 496 511	768 … . . . . . . …. 1023	1280 … . . . . . . … 1535	1792 .. . . … 2047	2304… . . . . . . … 2559	2816.. . . . . . . … 3071	3312 … 3326 3327 … . . . . 3537 … 3551	

Figure 7-3: Sequencing of bits within an input block

The encoder output consists of rectangular blocks of size (2 B) × N = 32 × 128 bits. The encoder output blocks are numbered 0, 1, 2, …. Bit k = 0, 1, 2, ... of row p in rectangle P is the bit {2P + [p/B], [p/B], k/B, p % B} of the semi-infinite array.

The bits within an output block are sequenced according to Figure 7-4.

0 1 … 15 16 17 … 31 32… . . . . 240 .. . 255	512… . . . . . . … 767	1024 … . . . . . . … 1279	1536 … . . . . . . … 1791	2048 … . . . . . . … 2303	2560 … . . . . . . … 2815	3072 . . . . . . … 3327	3584 . . . . . . … 3839
256… 271 272 . . . . 496 511	768 … . . . . . . …. 1023	1280 … . . . . . . … 1535	1792 .. . . … 2047	2304… . . . . . . … 2559	2816.. . . . . . . … 3071	3328 . . . . . . … 3583	3840 . . . . . . … 4095

Figure 7-4: Bit numbering within an output block

7.4 Formal encoder definition

This section directly describes the encoder (ENC0 or ENC1) output bits as a function of the input bits, integrating the diverse elements that have been described in previous sections.

An OFEC encoder is an entity that produces a binary output y(i) from a binary input u(i), where i = 0, 1, 2, ….

The relationship between y and u is expressed through intermediate variables.

In particular, there is a four dimensional array V(R, C, r, c), where R is an integer; C = 0, 1, …,7; r = 0, 1, …,15; and c = 0, 1, …, 15.

Associated with array V, there are constituent component codeword vectors $W_{R,rw}$ with elements $W_{R,r}(i)$, where R ≥ 0, r = 0, 1. 2….15, and i = 0, 1, …, 255.

$$\text{For } R \geq 0,\ W_{R,r}(k) = \begin{cases} V((R \wedge 1) - 20 + 2[k/16], [k/16], (k \,\%\, 16) \wedge r, r) \text{ for } k < 128 \\ V(R, [(k - 128)/16], r, (k \,\%\, 16) \wedge r) \text{ for } 128 \leq k < 256 \end{cases}$$

where,

[.] denotes the floor operator,

(a % b) denotes the value of a modulo b, and

(a ^ b) represents the number with a binary representation equal to the bitwise "exclusive or" of the binary representations of the numbers a and b.

The bits in the $W_{R,r}$ satisfy the following equalities:

For R ≥ 0, r = 0, 1, …, 15 and k = 0, 1, …, 110

WR,r(128 + k) = u([R/2] × 32 × 111 + ((R % 2) × 16 + r) × (16 – [k/96]) + [k/16] × 512 + k % 16)

For R ≥ 20, $W_{R,r}$ H = 0, where H is a parity check matrix of an extended *BCH*(256, 239) code, using a textbook encoding; i.e., if *x* is a vector satisfying *x*H = 0, then

1. x has an even parity, and
1. if the first 255 bits of x are seen as the binary coefficients of a polynomial x(t) of degree 254 (with bit 0 of x being the coefficient of power 254), with t being the indeterminate, then this binary polynomial x(t) is divisible by the binary codeword generator polynomial t16 + t14 + t13 + t11 + t10 + t9 + t8 + t6 +t5 + t +1.

The output y satisfies the relationship

For R ≥ 0; C = 0, 1, ..., 7; r = 0, 1, …, 15; and c = 0, 1, …, 15.

V (R, C, r, c) = y([R/2] × 32 × 128 + (R % 2) × 256 + C × 16 × 32 + r × 16 + c)

It can be observed that 20 × 16 ×17 values are left undefined in $W_{R,r}$ and in V(R, C, r, c) for 0 ≤ R < 20, and thus also in the output y. This is by design; an implementation can choose any convenient values. Interoperability between compliant implementations is not affected whatever values are used.

However, for test vectors, the output needs to be totally specified. To that end, the following additional constraints are added for designs that will use the test vectors for verification:

For $0 \leq R < 20$, $W_{R,r}$ H' = 0, where H' is a 256 × 17 binary matrix where the first 128 rows are all zero and the last 128 rows are equal to the last 128 rows of H.

7.5 Decoding

Any of the iterative algorithms designed for turbo decoding of Product Codes can easily be adapted to decode OFEC codewords.

For use with iterative decoding, observe that the bits in square block row will all have been decoded as front bits in later constituent component codewords after 2 (N/B + G + 1) rows of blocks have been decoded. Specifically, in Figure 7-2, bits in square block row R = 0 will all have been decoded as front bits by the time block row 21 has been decoded. It then makes sense to decode the constituent component codewords in block row 0 again.

7.6 OFEC Interleaver

The FEC datapath is shown in Figure 7-1. After OFEC encoding, mapping the bit stream is interleaved by a block interleaver. The interleaver block size is 172,032 bits (42 encoder output blocks, 21 from ENC0 and 21 from ENC1). The number of interleaver blocks per ZRx-OFEC structure is dependent on the modulation:

- DP-16QAM = (1376256/172032) = 8
- DP-8QAM = (1032192/172032) = 6
- DP-QPSK = (688128/172032) = 4

7.7 OFEC Interleaver architecture

The 172,032 bits in an interleaver block are organized as an (84, 8) array of 16 bit × 16-bit square blocks; see Figure 7-5 below. Note that the format is like the format used by the encoder and decoder. We then apply the two following mechanisms:

1. An intra-block interleaver that reorders the bits in each 16×16 square block to ensure that the bits in each row and column of a square block at the encoder output are remapped almost uniformly in the square block for transmission on the line. That operation can be seen as happening on input to the interleaver.
2. An inter-block interleaver that attempts to have nearby symbols on the line contain bits that are widely separated in the encoder output.

The interleaver is full rate, but it is fed by two half rate encoders, ENC0 and ENC1. Successive rows of square blocks from ENC0 will be written in even block rows of the interleaver buffer (yellowish colors in Figure 7-5), whereas successive rows of square blocks from ENC1 will be written in odd block rows (pinkish colors). Consequently, the content of an interleaver buffer is the square block row by square block row interleaving of vertical segments of the semi-infinite matrices of encoders ENC0 and ENC1.

7.8 Intra-block interleaving

For intra-block interleaving, the interleaver is considered to receive 16 × 16 square blocks of bits from the encoders, and each square block is considered separately.

The intra-block interleaving is specified by the following Table 7-1, which indicates the row and column of the source bit for each destination bit in the square block. For example,

bit (14, 15) [base 0] encoder output block is placed in row 1 of column 0 of the corresponding interleaver square block.

0,0	1,1	2,2	3,3	4,4	5,5	6,6	7,7	8,8	9,9	10,10	11,11	12,12	13,13	14,14	15,15
14,15	15,0	0,1	1,2	2,3	3,4	4,5	5,6	6,7	7,8	8,9	9,10	10,11	11,12	12,13	13,14
12,14	13,15	14,0	15,1	0,2	1,3	2,4	3,5	4,6	5,7	6,8	7,9	8,10	9,11	10,12	11,13
10,13	11,14	12,15	13,0	14,1	15,2	0,3	1,4	2,5	3,6	4,7	5,8	6,9	7,10	8,11	9,12
8,12	9,13	10,14	11,15	12,0	13,1	14,2	15,3	0,4	1,5	2,6	3,7	4,8	5,9	6,10	7,11
6,11	7,12	8,13	9,14	10,15	11,0	12,1	13,2	14,3	15,4	0,5	1,6	2,7	3,8	4,9	5,10
4,10	5,11	6,12	7,13	8,14	9,15	10,0	11,1	12,2	13,3	14,4	15,5	0,6	1,7	2,8	3,9
2,9	3,10	4,11	5,12	6,13	7,14	8,15	9,0	10,1	11,2	12,3	13,4	14,5	15,6	0,7	1,8
15,7	0,8	1,9	2,10	3,11	4,12	5,13	6,14	7,15	8,0	9,1	10,2	11,3	12,4	13,5	14,6
13,6	14,7	15,8	0,9	1,10	2,11	3,12	4,13	5,14	6,15	7,0	8,1	9,2	10,3	11,4	12,5
11,5	12,6	13,7	14,8	15,9	0,10	1,11	2,12	3,13	4,14	5,15	6,0	7,1	8,2	9,3	10,4
9,4	10,5	11,6	12,7	13,8	14,9	15,10	0,11	1,12	2,13	3,14	4,15	5,0	6,1	7,2	8,3
7,3	8,4	9,5	10,6	11,7	12,8	13,9	14,10	15,11	0,12	1,13	2,14	3,15	4,0	5,1	6,2
5,2	6,3	7,4	8,5	9,6	10,7	11,8	12,9	13,10	14,11	15,12	0,13	1,14	2,15	3,0	4,1
3,1	4,2	5,3	6,4	7,5	8,6	9,7	10,8	11,9	12,10	13,11	14,12	15,13	0,14	1,15	2,0
1,0	2,1	3,2	4,3	5,4	6,5	7,6	8,7	9,8	10,9	11,10	12,11	13,12	14,13	15,14	0,15

Table 7-1: Source positions (row, col) for intra-block interleaving

Note: The left entries of the pairs in this table form a Latin Square. The right entries almost form a Latin square, but they are duplicated in the first and last rows.

7.9 Inter-block interleaving

The intra-block permutation described in the previous section is applied to each square block in the buffer as it comes in from the encoder.

In addition to partitioning the interleaver buffer as a function of the encoder, ENC0 or ENC1, it is also partitioned in an upper half of 42 block rows (light color tones) and a lower half of 42 block rows (dark color tones). Overall, the buffer is then partitioned in 4 subsets, each containing 21 × 8 square blocks or 336 × 128 bits.

Subset number	Row Blocks
0	0, 2, …, 40
1	1, 3, …, 41
2	42, 44, …, 82
3	43, 45, …, 83

Table 7-2: Interleaver subsets

On output, groups of 8 bits are taken in turn from each subset, reading them out of a column of bits before proceeding to the next columns of bits. These output bits form the FlexO-x-DO structure.

Specifically, as shown in Figure 7-5, the first 8 bits are read from the top of first column of subset 0, then the first 8 bits from the first column of subsets 1, 2, and 3. Those 32 bits are

then followed by the taking the next 8 bits in the first column of each of the subsets 0, 1, 2, and 3. After 42 such cycles of 4 × 8 bits each, the first bit column of the interleaver buffer will be completely read out, and the output process continues by reading bit columns 1 to 127.

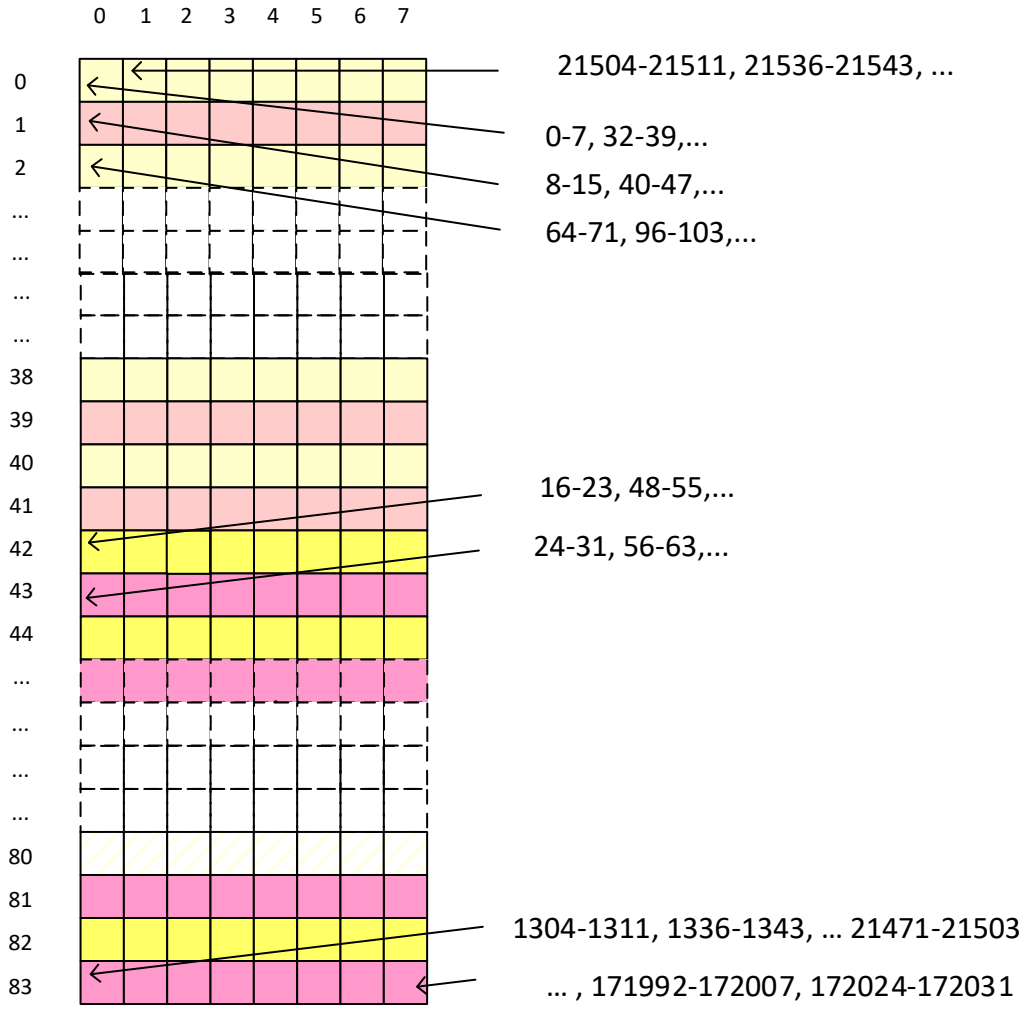


Figure 7-5: Inter-block interleaving

Note: Bits are read by columns, rather than rows because interleaver columns are much longer than rows, so bits in a column are spread over more constituent component codewords than bits in a row, which increases the tolerance to long bursts. The maximum correctable burst length, when used with a hard decoder, is a traditional measure of interleaver quality. In this case it can be shown to be 2,681 bits.

The bits read out of the interleaver are passed to the modulator where they are used in groups of S = 4, 6 or 8, for QPSK, 8QAM and 16QAM respectively in both the H and V polarizations.

Note: The output bits with even indexes are used to form symbols for the H polarization, whereas those in odd positions are formed to symbols in the V polarization. This simplifies the line BER estimation in each polarization. The H and V bits will appear at fixed positions in each square block in the decoder independently of the modulation.

8 Symbol Mapping and Polarization Distribution

This section describes the procedure for mapping encoded and interleaved OFEC Blocks to DP-QPSK and DP-nQAM constellation symbols for distribution on each (X/Y) polarizations. This procedure is illustrated in Figure 8-1 below.

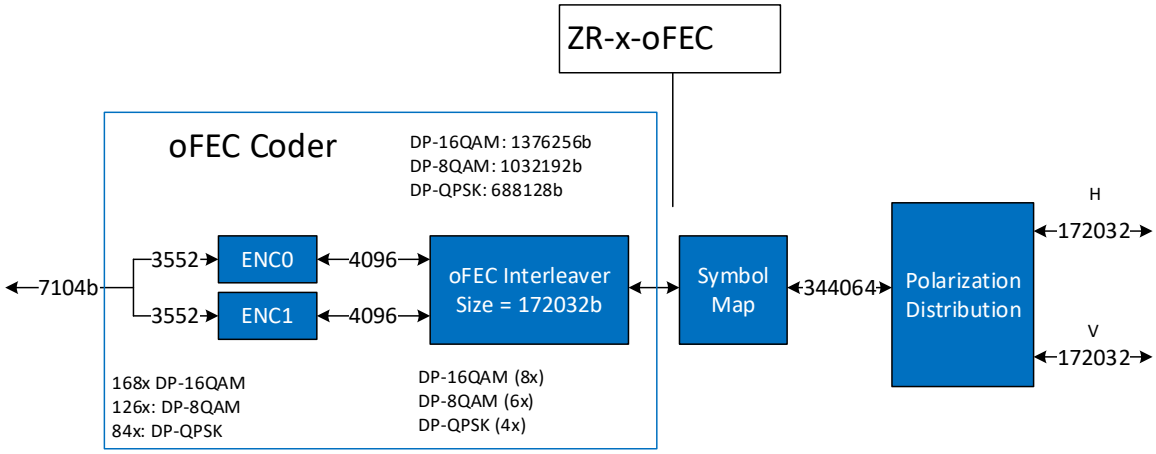


Figure 8-1: DSP symbol mapping and polarization distribution

8.1 Symbol mapping

Symbol mapping is modulation dependent. Each ZRx-OFEC structure is mapped to 172032 symbols in each polarization.

8.2 DP-16QAM Symbols

The ZR400-OFEC bits denoted by c_k (k=0…1376255) are mapped to 16QAM symbols (S).

$\boldsymbol{S} = [\boldsymbol{s_0}, \boldsymbol{s_1}, \ldots, \boldsymbol{s_{172031}}]$,

where,

$(\boldsymbol{c_{8i}}, \boldsymbol{c_{8i+2}})$ maps to the in-phase (I) component of the X-pol of $\boldsymbol{s_i}$

$(\boldsymbol{c_{8i+4}}, \boldsymbol{c_{8i+6}})$ maps to the quadrature-phase (Q) component of the X-pol of $\boldsymbol{s_i}$

$(\boldsymbol{c_{8i+1}}, \boldsymbol{c_{8i+3}})$ maps to the I component of the Y-pol of $\boldsymbol{s_i}$

$(\boldsymbol{c_{8i+5}}, \boldsymbol{c_{8i+7}})$ maps to the Q component of the Y-pol of $\boldsymbol{s_i}$

In each signaling dimension, the following mapping from binary label to relative symbol amplitude is defined as:

(0,0) →–3, (0,1) → –1, (1,1) →+1, (1,0) →+3

This mapping per polarization is further detailed in Table 8-1 below.

$(c_{8i}, c_{8i+2}, c_{8i+4}, c_{8i+6})$ *or* $(c_{8i+1}, c_{8i+3}, c_{8i+5}, c_{8i+7})$	I	Q
(0,0,0,0)	–3	–3
(0,0,0,1)	–3	–1
(0,0,1,0)	–3	3
(0,0,1,1)	–3	1
(0,1,0,0)	–1	–3
(0,1,0,1)	–1	–1
(0,1,1,0)	–1	3
(0,1,1,1)	–1	1
(1,0,0,0)	3	–3
(1,0,0,1)	3	–1
(1,0,1,0)	3	3
(1,0,1,1)	3	1
(1,1,0,0)	1	–3
(1,1,0,1)	1	–1
(1,1,1,0)	1	3
(1,1,1,1)	1	1

Table 8-1: 16QAM symbol amplitude map

8.3 8QAM Symbols

The ZR300-OFEC bits denoted by c_k (k=0…1032191) are mapped to 8QAM symbols (S),

$$\boldsymbol{S} = [\boldsymbol{s_0}, \boldsymbol{s_1}, \ldots, \boldsymbol{s_{172031}}]$$

where,

$(\boldsymbol{c_{6i}}, \boldsymbol{c_{6i+2}}, \boldsymbol{c_{6i+4}})$ maps to the in-phase/quadrature-phase (I/Q) component of the X-pol of $\boldsymbol{s_i}$

$(\boldsymbol{c_{6i+1}}, \boldsymbol{c_{6i+3}}, \boldsymbol{c_{6i+5}})$ maps to the I/Q component of the Y-pol of $\boldsymbol{s_i}$

In each polarization, we define the following map from binary label to relative symbol amplitudes:

$(c_{6i}, c_{6i+2}, c_{6i+4})$ *or* $(c_{6i+1}, c_{6i+3}, c_{6i+5})$	I	Q
(0,0,0)	0	-1
(0,0,1)	-1.366	-1.366
(0,1,0)	-1.366	1.366
(0,1,1)	-1	0
(1,0,0)	1.366	-1.366
(1,0,1)	1	0
(1,1,0)	0	1
(1,1,1)	1.366	1.366

Table 8-2: 8QAM symbol amplitude map

8.4 QPSK Symbols

The ZR200-OFEC or ZR100-OFEC bits denoted by c_k (k=0…688127) are mapped to QPSK symbols (S),

$$\boldsymbol{S = [s_0, s_1, \ldots, s_{172031}]}$$

where,

$(\boldsymbol{c_{4i}})$ maps to the in-phase (I) component of the X-pol of $\boldsymbol{s_i}$

$(\boldsymbol{c_{4i+2}})$ maps to the quadrature-phase (Q) component of the X-pol of $\boldsymbol{s_i}$

$(\boldsymbol{c_{4i+1}})$ maps to the I component of the Y-pol of $\boldsymbol{s_i}$

$(\boldsymbol{c_{4i+3}})$ maps to the Q component of the Y-pol of $\boldsymbol{s_i}$

In each polarization, we define the following map from binary label to relative symbol amplitudes:

(c_{4i}, c_{4i+2}) *or* (c_{4i+1}, c_{4i+3})	I	Q
(0,0)	-1	-1
(0,1)	-1	1
(1,0)	1	-1
(1,1)	1	1

Table 8-3: QPSK symbol amplitude map

9 DSP Framing

This section describes the DSP framing format. The DSP super-frame consists of 48 DSP sub-frames. The DSP frame length expressed in symbols is modulation independent. The frame format is defined for each polarization (X/Y).

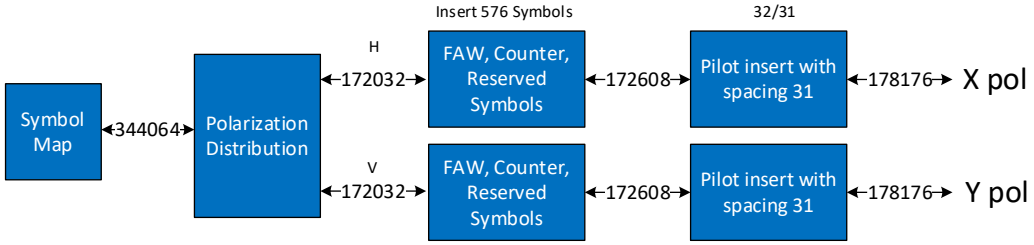


Figure 9-1: DSP Frame generation

9.1 DSP super-frame

A DSP super-frame is defined as a set of 178176 symbols in each X/Y polarization. A DSP sub-frame consists of 3712 symbols. The DSP super-frame thus consists of 48 DSP sub-frames.

Pilot Symbols (PS) are inserted every 32 symbols starting with the first symbol of the first DSP sub-frame. Each DSP sub-frame starts with an 11-symbol training sequence. The first symbol of the training sequence is a Pilot Symbol. The first DSP sub-frame of the super-frame also includes the DSP super-frame Frame Alignment Word (FAW).

As illustrated in Figure 9-1 above, once the data stream has been mapped into symbols and distributed onto each polarization pilot symbols, training symbols, Frame Alignment Word (FAW), and other overhead are added to create the DSP super-frame/sub-frame structure. Pilot symbols, Training symbols, and FAW symbols are always mapped to the outer constellation points of the optical signal.

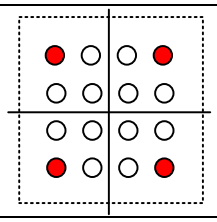
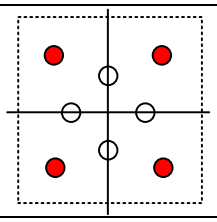
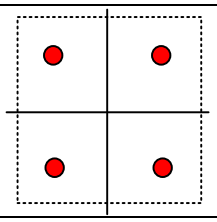
Parameter	DP-16QAM	DP-8QAM	DP-QPSK
Constellation Map			
FAW	22 Symbols	22 Symbols	22 Symbols
TS	11 symbols per DSP sub-frame	11 symbols per DSP sub-frame	11 symbols per DSP sub-frame
PS	Every 32 symbols	Every 32 symbols	Every 32 symbols

Table 9-1: FAW/TS/PS pattern

9.2 DSP sub-frame

Each DSP super-frame is divided into 48 DSP sub-frames and each DSP sub-frame consists of 3,712 symbols.

The first DSP sub-frame of the DSP super-frame includes a 22 symbol Frame Alignment Word (FAW) used for alignment to the OFEC blocks. 74 additional symbols are reserved for future use/innovation.

The first DSP sub-frame includes:

- 22 symbol super-frame Frame Alignment Word (FAW) used for super-frame delineation and alignment to the OFEC block. 74 additional symbols are reserved for future use/innovation. The FAW sequence is different between X and Y polarizations.
- 74 symbols are reserved to be used for future proofing and for innovation. These symbols should be randomized to avoid strong tones.
- 11 symbols available for link training. The first Training Symbol (TS) is shared as a Pilot Symbol (PS) in each DSP sub-frame.
- 116 Pilot Symbols.

Every subsequent DSP sub-frame (sub-frames 2-48 of a DSP super-frame) include:

- 11 symbols available for link training. The first Training Symbol (TS) is shared as a Pilot Symbol (PS) in each DSP sub-frame.
- 116 Pilot Symbols

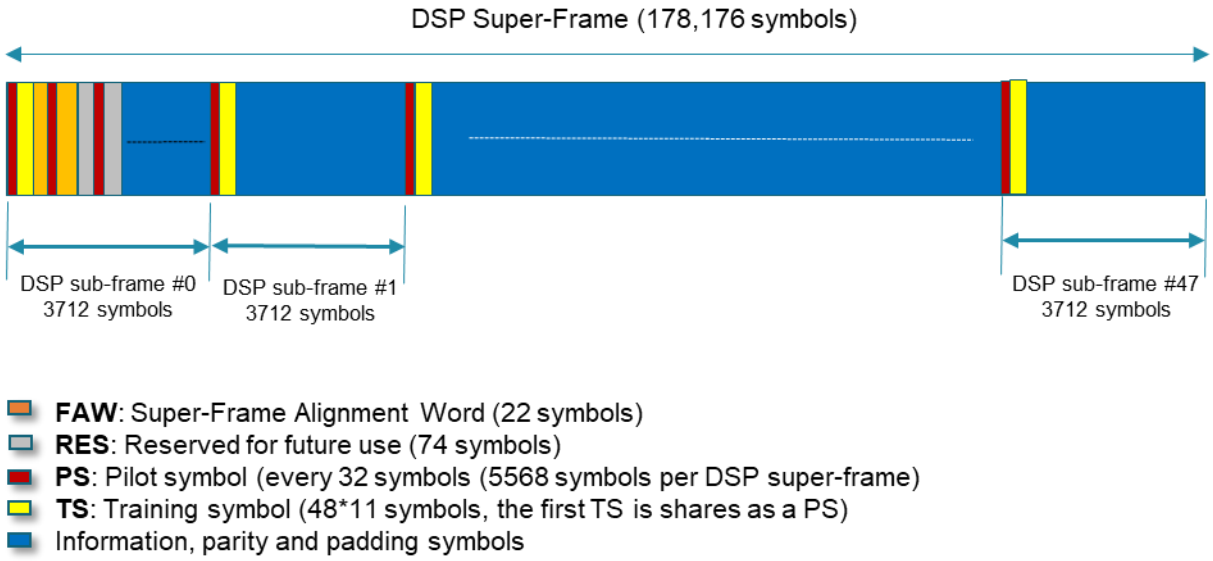


Figure 9-2: DSP super-frame

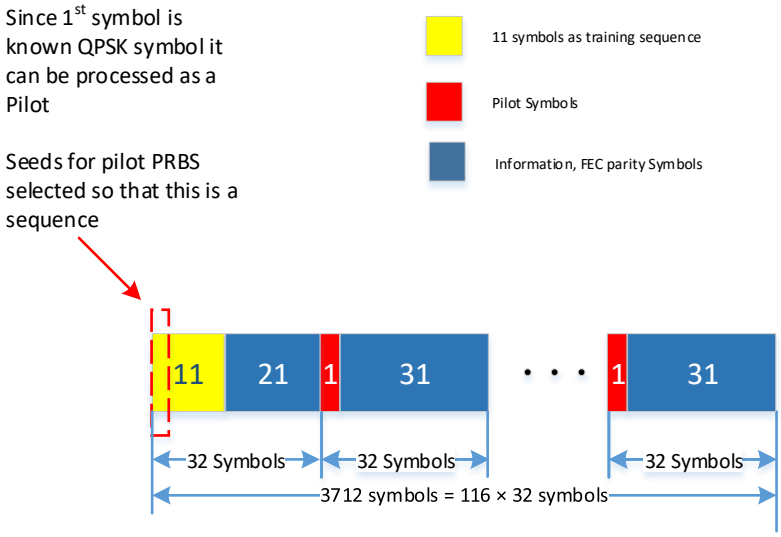


Figure 9-3: DSP sub-frames 1 to 47 of the DSP super-frame

9.3 FAW Sequence

The required sequence and constellation corner relative symbol amplitude for the 16QAM FAW is shown in Table 9-2.

	16QAM		8QAM		QPSK	
Index	**FAW (X)**	**FAW (Y)**	**FAW (X)**	**FAW (Y)**	**FAW (X)**	**FAW (Y)**
1	3–3j	3+3j	1.366–1.366j	1.366+1.366j	1–1j	1+1j
2	3+3j	–3+3j	1.366+1.366j	–1.366+1.366j	1+1j	–1+1j
3	3+3j	–3–3j	1.366+1.366j	–1.366–1.366j	1+1j	–1–1j
4	3+3j	–3+3j	1.366+1.366j	–1.366+1.366j	1+1j	–1+1j
5	3 –3j	3 –3j	1.366 –1.366j	1.366 –1.366j	1 –1j	1 –1j
6	3 –3j	3+3j	1.366 –1.366j	1.366+1.366j	1 –1j	1+1j
7	–3 –3j	3 –3j	–1.366 –1.366j	1.366 –1.366j	–1 –1j	1 –1j
8	3+3j	3 –3j	1.366+1.366j	1.366 –1.366j	1+1j	1 –1j
9	–3 –3j	–3 –3j	–1.366 –1.366j	–1.366 –1.366j	–1 –1j	–1 –1j
10	–3+3j	3 –3j	–1.366+1.366j	1.366 –1.366j	–1+1j	1 –1j
11	–3+3j	3+3j	–1.366+1.366j	1.366+1.366j	–1+1j	1+1j
12	3 –3j	–3+3j	1.366 –1.366j	–1.366+1.366j	1 –1j	–1+1j
13	–3 –3j	–3+3j	–1.366 –1.366j	–1.366+1.366j	–1 –1j	–1+1j
14	–3 –3j	3+3j	–1.366 –1.366j	1.366+1.366j	–1 –1j	1+1j
15	–3+3j	–3 –3j	–1.366+1.366j	–1.366 –1.366j	–1+1j	–1 –1j
16	3+3j	3+3j	1.366+1.366j	1.366+1.366j	1+1j	1+1j
17	–3 –3j	–3 –3j	–1.366 –1.366j	–1.366 –1.366j	–1 –1j	–1 –1j
18	3 –3j	–3+3j	1.366 –1.366j	–1.366+1.366j	1 –1j	–1+1j
19	–3+3j	3 –3j	–1.366+1.366j	1.366 –1.366j	–1+1j	1 –1j
20	3+3j	–3 –3j	1.366+1.366j	–1.366 –1.366j	1+1j	–1 –1j
21	–3 –3j	3 –3j	–1.366 –1.366j	1.366 –1.366j	–1 –1j	1 –1j
22	–3+3j	–3+3j	–1.366+1.366j	–1.366+1.366j	–1+1j	–1+1j

Table 9-2: FAW Sequence

9.4 Training Sequence

The required sequence and constellation corner relative symbol amplitude for the 16QAM TS is shown in Table 9-3. The constellation corner relative symbol amplitude for the 8QAM TS and QPSK TS should be scaled per Table 8-2 and Table 8-3 respectively.

	16QAM		8QAM		QPSK	
Index	**Training (X)**	**Training (Y)**	**Training (X)**	**Training (Y)**	**Training (X)**	**Training (Y)**
1*	–3+3j	–3 –3j	–1.366+1.366j	–1.366 –1.366j	–1+1j	–1 –1j
2	3+3j	–3 –3j	1.366+1.366j	–1.366 –1.366j	1+1j	–1 –1j
3	–3+3j	3 –3j	–1.366+1.366j	1.366 –1.366j	–1+1j	1 –1j
4	3+3j	–3+3j	1.366+1.366j	–1.366+1.366j	1+1j	–1+1j
5	–3 –3j	–3+3j	–1.366 –1.366j	–1.366+1.366j	–1 –1j	–1+1j
6	3+3j	3+3j	1.366+1.366j	1.366+1.366j	1+1j	1+1j
7	–3 –3j	–3 –3j	–1.366 –1.366j	–1.366 –1.366j	–1 –1j	–1 –1j
8	–3 –3j	–3+3j	–1.366 –1.366j	–1.366+1.366j	–1 –1j	–1+1j
9	3+3j	3 –3j	1.366+1.366j	1.366 –1.366j	1+1j	1 –1j
10	3 –3j	3+3j	1.366 –1.366j	1.366+1.366j	1 –1j	1+1j
11	3 –3j	3 –3j	1.366 –1.366j	1.366 –1.366j	1 –1j	1 –1j

Table 9-3: Training symbol sequence

*The first symbol of the Training Sequence is processed as a pilot

9.5 Pilot Sequence

Training symbols and pilot symbols shall be set at the outer 4 points of the DP-nQAM constellation.

The Pilot is a fixed PRBS10 mapped to the QPSK sequence with different seed values for X/Y.

- Seeds are selected so that pilots are DC balanced
- Seeds are selected so that the 1st symbol in the training sequence is also the first symbol in the pilot sequence
- The seed is reset at the head of every DSP super-frame

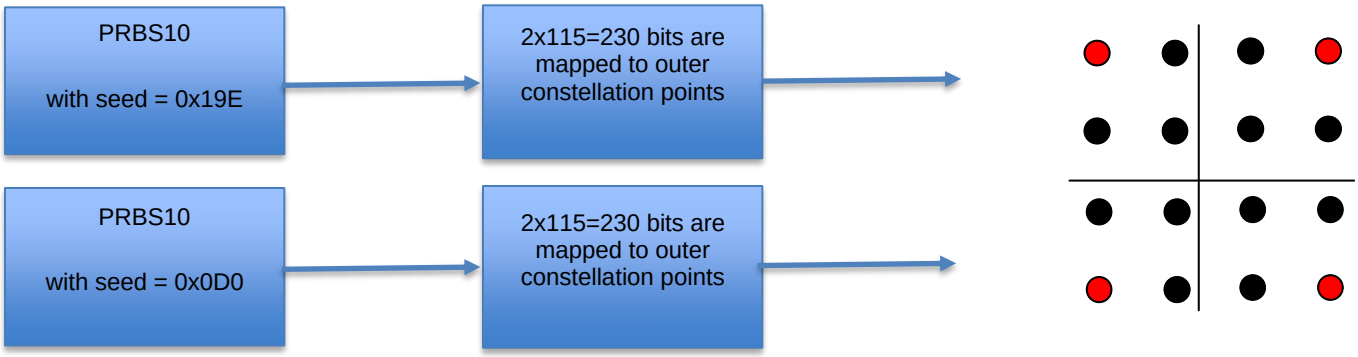


Figure 9-4: Pilot Symbol (DP-16QAM modulation shown)

Generator polynomial	Seed X	Seed Y
$x^{10} + x^8 + x^4 + x^3 + 1$	0x19E	0x0D0

Table 9-4: Pilot Sequence

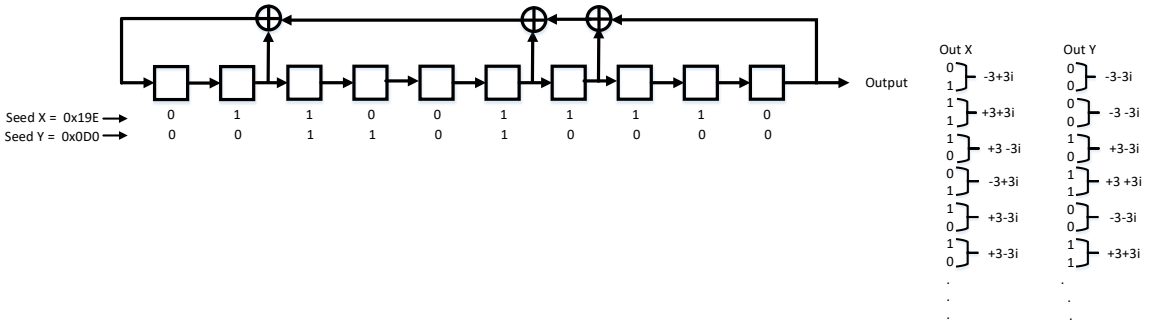


Figure 9-5: Pilot Seed and Sequencing

The required sequence and constellation corner relative symbol amplitude for the 16QAM PS is shown in Table 9-5. The constellation corner relative symbol amplitude for the 8QAM PS and QPSK PS should be scaled per Table 8-2 and Table 8-3 respectively.

The complete table is in Table 9-5.

	16QAM		8QAM		QPSK	
Index	**Pilot X**	**Pilot Y**	**Pilot X**	**Pilot Y**	**Pilot X**	**Pilot Y**
1	–3+3i	–3 –3i	–1.366+1.366i	–1.366 –1.366i	–1+1i	–1 –1i
2	3+3i	–3 –3i	1.366+1.366i	–1.366 –1.366i	1+1i	–1 –1i
3	3 –3i	3 –3i	1.366 –1.366i	1.366 –1.366i	1 –1i	1 –1i
4	–3+3i	3+3i	–1.366+1.366i	1.366+1.366i	–1+1i	1+1i
5	3 –3i	–3 –3i	1.366 –1.366i	–1.366 –1.366i	1 –1i	–1 –1i
6	3 –3i	3+3i	1.366 –1.366i	1.366+1.366i	1 –1i	1+1i
7	–3 –3i	–3+3i	–1.366 –1.366i	–1.366+1.366i	–1 –1i	–1+1i
8	3+3i	–3+3i	1.366+1.366i	–1.366+1.366i	1+1i	–1+1i
9	–3+3i	–3 –3i	–1.366+1.366i	–1.366 –1.366i	–1+1i	–1 –1i
10	3+3i	3+3i	1.366+1.366i	1.366+1.366i	1+1i	1+1i
11	3+3i	3+3i	1.366+1.366i	1.366+1.366i	1+1i	1+1i
12	–3 –3i	–3 –3i	–1.366 –1.366i	–1.366 –1.366i	–1 –1i	–1 –1i
13	3+3i	3+3i	1.366+1.366i	1.366+1.366i	1+1i	1+1i
14	3 –3i	3+3i	1.366 –1.366i	1.366+1.366i	1 –1i	1+1i
15	3+3i	3 –3i	1.366+1.366i	1.366 –1.366i	1+1i	1 –1i
16	3 –3i	3+3i	1.366 –1.366i	1.366+1.366i	1 –1i	1+1i
17	3+3i	3+3i	1.366+1.366i	1.366+1.366i	1+1i	1+1i
18	3 –3i	–3+3i	1.366 –1.366i	–1.366+1.366i	1 –1i	–1+1i
19	–3+3i	–3 –3i	–1.366+1.366i	–1.366 –1.366i	–1+1i	–1 –1i
20	–3 –3i	3 –3i	–1.366 –1.366i	1.366 –1.366i	–1 –1i	1 –1i
21	3+3i	3 –3i	1.366+1.366i	1.366 –1.366i	1+1i	1 –1i
22	–3+3i	3+3i	–1.366+1.366i	1.366+1.366i	–1+1i	1+1i
23	–3+3i	–3+3i	–1.366+1.366i	–1.366+1.366i	–1+1i	–1+1i
24	3 –3i	3 –3i	1.366 –1.366i	1.366 –1.366i	1 –1i	1 –1i
25	–3+3i	3 –3i	–1.366+1.366i	1.366 –1.366i	–1+1i	1 –1i
26	–3+3i	3+3i	–1.366+1.366i	1.366+1.366i	–1+1i	1+1i
27	–3+3i	–3+3i	–1.366+1.366i	–1.366+1.366i	–1+1i	–1+1i
28	–3+3i	3+3i	–1.366+1.366i	1.366+1.366i	–1+1i	1+1i
29	–3 –3i	3+3i	–1.366 –1.366i	1.366+1.366i	–1 –1i	1+1i
30	3 –3i	3 –3i	1.366 –1.366i	1.366 –1.366i	1 –1i	1 –1i
31	–3 –3i	–3+3i	–1.366 –1.366i	–1.366+1.366i	–1 –1i	–1+1i
32	3+3i	–3 –3i	1.366+1.366i	–1.366 –1.366i	1+1i	–1 –1i
33	–3+3i	3 –3i	–1.366+1.366i	1.366 –1.366i	–1+1i	1 –1i
34	–3+3i	–3 –3i	–1.366+1.366i	–1.366 –1.366i	–1+1i	–1 –1i
35	–3+3i	–3 –3i	–1.366+1.366i	–1.366 –1.366i	–1+1i	–1 –1i
36	3 –3i	3 –3i	1.366 –1.366i	1.366 –1.366i	1 –1i	1 –1i
37	3 –3i	3 –3i	1.366 –1.366i	1.366 –1.366i	1 –1i	1 –1i
38	–3 –3i	–3 –3i	–1.366 –1.366i	–1.366 –1.366i	–1 –1i	–1 –1i
39	–3 –3i	3+3i	–1.366 –1.366i	1.366+1.366i	–1 –1i	1+1i

	16QAM		8QAM		QPSK	
Index	**Pilot X**	**Pilot Y**	**Pilot X**	**Pilot Y**	**Pilot X**	**Pilot Y**
40	3 –3i	–3 –3i	1.366 –1.366i	–1.366 –1.366i	1 –1i	–1 –1i
41	–3 –3i	3 –3i	–1.366 –1.366i	1.366 –1.366i	–1 –1i	1 –1i
42	3 –3i	3 –3i	1.366 –1.366i	1.366 –1.366i	1 –1i	1 –1i
43	–3+3i	–3 –3i	–1.366+1.366i	–1.366 –1.366i	–1+1i	–1 –1i
44	–3+3i	–3 –3i	–1.366+1.366i	–1.366 –1.366i	–1+1i	–1 –1i
45	–3 –3i	3+3i	–1.366 –1.366i	1.366+1.366i	–1 –1i	1+1i
46	–3+3i	–3+3i	–1.366+1.366i	–1.366+1.366i	–1+1i	–1+1i
47	–3 –3i	3+3i	–1.366 –1.366i	1.366+1.366i	–1 –1i	1+1i
48	3+3i	–3+3i	1.366+1.366i	–1.366+1.366i	1+1i	–1+1i
49	3+3i	3 –3i	1.366+1.366i	1.366 –1.366i	1+1i	1 –1i
50	–3+3i	–3+3i	–1.366+1.366i	–1.366+1.366i	–1+1i	–1+1i
51	3 –3i	3+3i	1.366 –1.366i	1.366+1.366i	1 –1i	1+1i
52	3 –3i	–3+3i	1.366 –1.366i	–1.366+1.366i	1 –1i	–1+1i
53	3 –3i	–3+3i	1.366 –1.366i	–1.366+1.366i	1 –1i	–1+1i
54	–3 –3i	3+3i	–1.366 –1.366i	1.366+1.366i	–1 –1i	1+1i
55	3 –3i	–3+3i	1.366 –1.366i	–1.366+1.366i	1 –1i	–1+1i
56	3+3i	–3+3i	1.366+1.366i	–1.366+1.366i	1+1i	–1+1i
57	–3+3i	–3 –3i	–1.366+1.366i	–1.366 –1.366i	–1+1i	–1 –1i
58	–3 –3i	3 –3i	–1.366 –1.366i	1.366 –1.366i	–1 –1i	1 –1i
59	3 –3i	3 –3i	1.366 –1.366i	1.366 –1.366i	1 –1i	1 –1i
60	3+3i	–3+3i	1.366+1.366i	–1.366+1.366i	1+1i	–1+1i
61	3 –3i	3+3i	1.366 –1.366i	1.366+1.366i	1 –1i	1+1i
62	–3 –3i	–3 –3i	–1.366 –1.366i	–1.366 –1.366i	–1 –1i	–1 –1i
63	3 –3i	3+3i	1.366 –1.366i	1.366+1.366i	1 –1i	1+1i
64	–3+3i	–3+3i	–1.366+1.366i	–1.366+1.366i	–1+1i	–1+1i
65	3 –3i	3 –3i	1.366 –1.366i	1.366 –1.366i	1 –1i	1 –1i
66	3+3i	3+3i	1.366+1.366i	1.366+1.366i	1+1i	1+1i
67	3 –3i	–3 –3i	1.366 –1.366i	–1.366 –1.366i	1 –1i	–1 –1i
68	–3+3i	3 –3i	–1.366+1.366i	1.366 –1.366i	–1+1i	1 –1i
69	3 –3i	–3+3i	1.366 –1.366i	–1.366+1.366i	1 –1i	–1+1i
70	–3+3i	–3+3i	–1.366+1.366i	–1.366+1.366i	–1+1i	–1+1i
71	3+3i	–3+3i	1.366+1.366i	–1.366+1.366i	1+1i	–1+1i
72	–3 –3i	–3 –3i	–1.366 –1.366i	–1.366 –1.366i	–1 –1i	–1 –1i
73	–3 –3i	–3+3i	–1.366 –1.366i	–1.366+1.366i	–1 –1i	–1+1i
74	3 –3i	3+3i	1.366 –1.366i	1.366+1.366i	1 –1i	1+1i
75	–3+3i	–3 –3i	–1.366+1.366i	–1.366 –1.366i	–1+1i	–1 –1i
76	3 –3i	–3 –3i	1.366 –1.366i	–1.366 –1.366i	1 –1i	–1 –1i
77	–3+3i	–3 –3i	–1.366+1.366i	–1.366 –1.366i	–1+1i	–1 –1i
78	–3 –3i	3+3i	–1.366 –1.366i	1.366+1.366i	–1 –1i	1+1i
79	3+3i	–3 –3i	1.366+1.366i	–1.366 –1.366i	1+1i	–1 –1i
80	3+3i	–3 –3i	1.366+1.366i	–1.366 –1.366i	1+1i	–1 –1i

	16QAM		8QAM		QPSK	
Index	**Pilot X**	**Pilot Y**	**Pilot X**	**Pilot Y**	**Pilot X**	**Pilot Y**
81	3+3i	3 –3i	1.366+1.366i	1.366 –1.366i	1+1i	1 –1i
82	–3 –3i	–3 –3i	–1.366 –1.366i	–1.366 –1.366i	–1 –1i	–1 –1i
83	–3 –3i	3+3i	–1.366 –1.366i	1.366+1.366i	–1 –1i	1+1i
84	3+3i	–3 –3i	1.366+1.366i	–1.366 –1.366i	1+1i	–1 –1i
85	3 –3i	–3 –3i	1.366 –1.366i	–1.366 –1.366i	1 –1i	–1 –1i
86	–3+3i	–3 –3i	–1.366+1.366i	–1.366 –1.366i	–1+1i	–1 –1i
87	3+3i	3 –3i	1.366+1.366i	1.366 –1.366i	1+1i	1 –1i
88	3 –3i	–3+3i	1.366 –1.366i	–1.366+1.366i	1 –1i	–1+1i
89	–3 –3i	–3+3i	–1.366 –1.366i	–1.366+1.366i	–1 –1i	–1+1i
90	3 –3i	3 –3i	1.366 –1.366i	1.366 –1.366i	1 –1i	1 –1i
91	3 –3i	3+3i	1.366 –1.366i	1.366+1.366i	1 –1i	1+1i
92	–3+3i	3 –3i	–1.366+1.366i	1.366 –1.366i	–1+1i	1 –1i
93	–3 –3i	3 –3i	–1.366 –1.366i	1.366 –1.366i	–1 –1i	1 –1i
94	3+3i	–3+3i	1.366+1.366i	–1.366+1.366i	1+1i	–1+1i
95	–3 –3i	3 –3i	–1.366 –1.366i	1.366 –1.366i	–1 –1i	1 –1i
96	–3 –3i	3 –3i	–1.366 –1.366i	1.366 –1.366i	–1 –1i	1 –1i
97	3+3i	–3+3i	1.366+1.366i	–1.366+1.366i	1+1i	–1+1i
98	–3+3i	3 –3i	–1.366+1.366i	1.366 –1.366i	–1+1i	1 –1i
99	3 –3i	–3 –3i	1.366 –1.366i	–1.366 –1.366i	1 –1i	–1 –1i
100	–3 –3i	3+3i	–1.366 –1.366i	1.366+1.366i	–1 –1i	1+1i
101	3+3i	–3 –3i	1.366+1.366i	–1.366 –1.366i	1+1i	–1 –1i
102	–3+3i	–3+3i	–1.366+1.366i	–1.366+1.366i	–1+1i	–1+1i
103	–3 –3i	–3+3i	–1.366 –1.366i	–1.366+1.366i	–1 –1i	–1+1i
104	–3 –3i	3+3i	–1.366 –1.366i	1.366+1.366i	–1 –1i	1+1i
105	3+3i	–3+3i	1.366+1.366i	–1.366+1.366i	1+1i	–1+1i
106	3 –3i	3 –3i	1.366 –1.366i	1.366 –1.366i	1 –1i	1 –1i
107	3+3i	3+3i	1.366+1.366i	1.366+1.366i	1+1i	1+1i
108	–3+3i	–3+3i	–1.366+1.366i	–1.366+1.366i	–1+1i	–1+1i
109	–3 –3i	3+3i	–1.366 –1.366i	1.366+1.366i	–1 –1i	1+1i
110	–3+3i	–3 –3i	–1.366+1.366i	–1.366 –1.366i	–1+1i	–1 –1i
111	–3 –3i	–3+3i	–1.366 –1.366i	–1.366+1.366i	–1 –1i	–1+1i
112	–3+3i	3 –3i	–1.366+1.366i	1.366 –1.366i	–1+1i	1 –1i
113	–3+3i	–3+3i	–1.366+1.366i	–1.366+1.366i	–1+1i	–1+1i
114	3+3i	3+3i	1.366+1.366i	1.366+1.366i	1+1i	1+1i
115	3+3i	3 –3i	1.366+1.366i	1.366 –1.366i	1+1i	1 –1i
116	–3 –3i	3 –3i	–1.366 –1.366i	1.366 –1.366i	–1 –1i	1 –1i

Table 9-5: Pilot Sequence

10 Frame Expansion Rate

The OFEC optical signal is ~ 60.138546798 GBd for ZR400, ZR300 and ZR200 rates and is ~ 30.069273399 GBd for ZR100 rate. Table 10-1 provides detail on expansion for each functional block.

Parameters	Mapping
FEC Payload	ZR100, ZR200, ZR300 or ZR400 frames
FEC algorithm	OFEC
FEC payload size (k)	3,552
FEC block size (n)	4,096
The number of FEC blocks in super frame	168(16QAM)/126(8QAM)/84(QPSK)
The total payload size	1,193,472(16QAM) 895,104(8QAM) 596,736(QPSK)
PAD before FEC	992(16QAM)/744(8QAM)/496(QPSK)
The total payload size based on 257b	1,192,480b (16QAM) 4,640×257b 894,360b (8QAM) 3,480×257b 596,240b (QPSK) 2,320×257b
The total bits	1,376,256(16QAM) 1,032,192(8QAM) 688,128(QPSK)
Total number of symbols per before DSP frame OH	172,032
The number of FAW symbols	22
The number of RES symbols	74
The number of Training Symbols	480
The number of Pilot Symbols (PS)	5,568
The total symbol of super-frame	178,176
DSP sub-frame symbols	3,712
The number of DSP sub-frames per super-frame	48
Modulation format	16QAM / 8QAM / QPSK
Baud rate	~60 138 546 798 Baud* or ~30 069 273 399 Baud for ZR100

Table 10-1: ZRx/OFEC expansion rates

*60.138546798 GBd = 401.703640510× (512/511) × (37296/37265) × (4096/3552) × (899/896) × (32/31) /8

11 Optical Specifications

The OpenZR+ optical parameters are provided in this section. Parameters for the DWDM link are requirements that ensure multi-vendor operation between compliant Tx / Rx modules.

Tx optical output parameters are measured at Ss, which is after a 2 to 5 m cable plugged into the module Tx output. Rx optical input parameters are measured at Rs, which is at the module Rx input. DWDM link parameters are measured between Ss inputs and Rs outputs. All specifications are defined after calibration and compensation, at end-of-life over temperature and wavelength.

11.1 DWDM link specifications

The parameters listed in Table 11-1 are the limits that can be supported by OpenZR+ transmitters and receivers. For operation on a 75 GHz grid spacing, links are required to limit crosstalk between channels by the characteristics of optical multiplexers and demultiplexers used in the link. An informative example of a compliant network is given in the appendix at section 13.

Ref.	Parameter	Mode	Min	Max	Unit	Conditions / Comments
11.1.100	Channel frequency	All	191.3	196.1	THz	
11.1.110	Channel spacing	All	75	—	GHz	
11.1.130	Fiber type	All				Single mode fiber per ITU-T G.652 used for link budgeting.
11.1.160	Chromatic dispersion	400G	—	20,000	ps/nm	Frequency dependent change in phase velocity due to fiber.
		300G	—	40,000		
		200G	—	50,000		
		100G	—	100,000		
11.1.161	Optical return loss at Ss	All	—	24	dB	
11.1.162	Discrete reflectance between Ss and Rs	All	—	-27	dB	
11.1.170	Instantaneous differential group delay (DGD)	400G	—	50	ps	The DGD max limits are based on a DGDmax to DGDmean ratio of 3.3 and are the fiber portion of the receiver PMD tolerance limits.
		300G	—	66		
		200G	—	66		
		100G	—	83		
11.1.171	Polarization dependent loss (PDL)	All	—	2	dB	
11.1.172	Polarization rotation speed	All	—	50	krad/s	

Table 11-1: Optical channel specifications

11.2 Transmitter Optical Specifications

Ref	Parameter	Line Rate	Min	Max	Unit	Conditions/Comments
	Modulation format	400G	DP-16QAM			
		300G	DP-8QAM			
		200G	DP-QPSK			
		100G	DP-QPSK			
	Baud rate	400G/300G/ 200G	60.138547 ± 20 ppm		GBd	
		100G	30.069274 ± 20 ppm			
11.1.200	Laser frequency accuracy	All	–1.8	1.8	GHz	
11.1.210	Laser frequency noise	All	—	See mask	Hz^2/Hz	See Figure 11-1
11.1.211	Laser RIN (average)	All	—	–145	dB/Hz	0.2 GHz ≤ f ≤ 10 GHz
11.1.212	Laser RIN (peak)	All	—	–140	dB/Hz	0.2 GHz ≤ f ≤ 10 GHz
11.1.213a	Tx clock low-frequency phase noise	All	—	see mask	dBc/Hz	See 11.2.1
11.1.213b	Tx clock total integrated RMS phase jitter	All	—	600	fs	10 kHz to 10 MHz
			—	250	fs	1 MHz to 200 MHz
11.1.215a	Tx spectral upper mask	All	—	(30.0, 0.0) (37.0, -10.0) (-39.2, -15.0) (-40.4, -20.0)	(GHz, dB)	See 11.4.10 for definition and mask
11.1.215b	Tx spectral lower mask	All	(30.0, -9.0) (31.3, -20.0) (31.3, -35.0)	—	(GHz, dB)	See 11.4.10 for definition and mask
11.1.220	Minimum Tx output signal power	400G	–10	—	dBm	Over wavelength, temperature, and aging.
		300G	–10	—		
		200G	–9	—		
		100G	–8	—		
11.1.220a	Tx output power stability		–1	+1	dB	Output power stability over life at a fixed wavelength
11.1.220b	Minimum provisionable Tx output power range	400G	–13	–9	dBm	For transmitters with adjustable power, the minimum range shall meet these limits.
11.1.220c	Tx power setting accuracy	All	–1	+1	dB	
11.1.221	Tx output power with transmit disabled	All	—	–20	dBm	
11.1.222	Total output power during wavelength switching	All	—	–20	dBm	
11.1.230	In-band (IB) OSNR	All	34	—	dB/0.1 nm	Tx signal power between the -20 dB Tx spectral mask frequency points, referenced to an optical noise bandwidth of 0.1 nm at 193.7 THz, or 12.5 GHz at the Tx peak signal frequency.

Ref	Parameter	Line Rate	Min	Max	Unit	Conditions/Comments
11.1.231	Out-of-band (OOB) OSNR	All	23	—	dB/0.1 nm	Tx signal power between the -20 dB Tx spectral mask frequency points, referenced to the maximum optical noise power within any optical bandwidth of 0.1 nm at 193.7 THz, or 12.5 GHz outside of the -20 dB Tx spectral mask.
11.1.240	Transmitter reflectance	All	—	–20	dB	Looking into the Tx
11.1.241	Transmitter back reflection tolerance	All	—	–24	dB	
11.1.250	Transmitter polarization dependent power difference	All	—	1.5	dB	Between X and Y polarization.
11.1.260	X-Y skew	All	—	5	ps	
11.1.270a	DC IQ_{offset}	All	—	–26	dB	Per polarization. See 11.4.8.
11.1.270b	I-Q instantaneous offset	All	—	–20	dB	Per polarization. See 11.4.8.
11.1.271	Mean I-Q amplitude imbalance	All	—	1	dB	
11.1.272	I-Q phase imbalance	All	–5	5	degrees	
11.1.273	I-Q skew	All	—	0.75	ps	

Table 11-2: Tx optical specifications

11.2.1 Laser maximum frequency noise mask

The measurement resolution bandwidth shall be between 10^{-1} and 10^{-6} times the frequency of interest. The high frequency component (100 MHz and above) of the phase noise is consistent with a 500 kHz laser line width. The receiver local oscillator has the same line width.

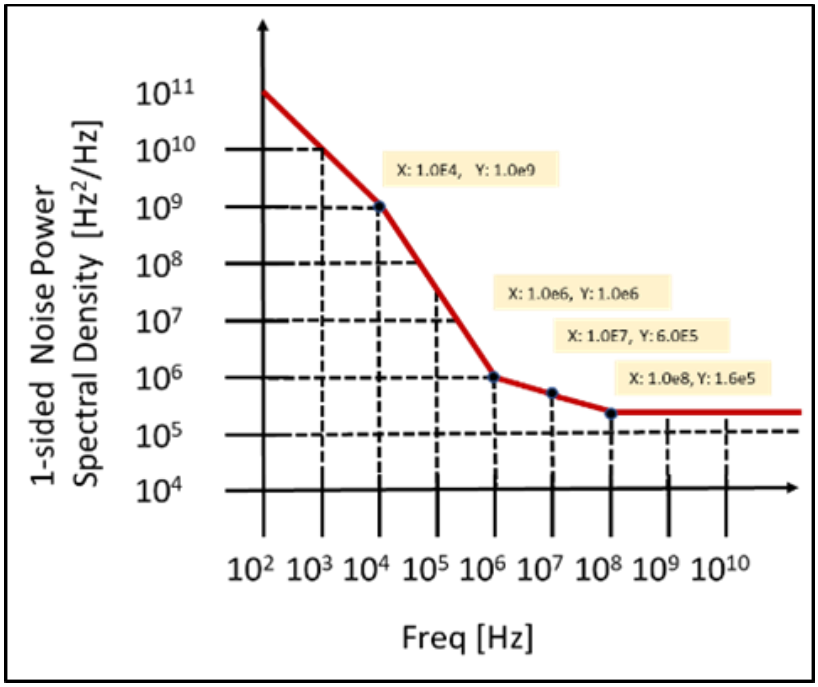


Figure 11-1 Laser maximum frequency noise mask

Table 11-3 Laser maximum frequency noise values at selected frequencies

Frequency [Hz]	1- sided Noise power spectral density [Hz²/Hz]
1.0e+02	1.0e+11
1.0e+04	1.0e+09
1.0e+06	1.0e+06
1.0e+07	6.0e+05
1.0e+08	1.6e+05
1.0e+09	1.6e+05

11.2.2 Tx clock maximum phase noise mask

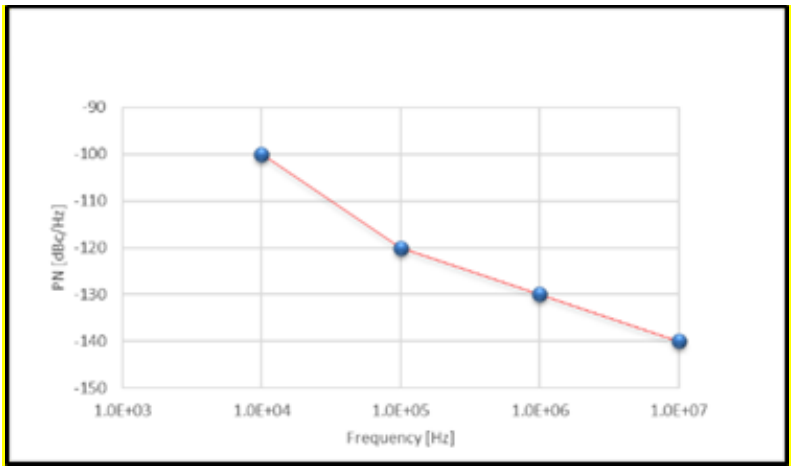


Figure 11-2 Tx clock phase noise mask at 469.83 MHz

Table 11-4 Phase noise in dBc/Hz versus frequency offset (Hz)

PN [dBc/Hz]	Frequency [Hz]
-100	1.00E+04
-120	1.00E+05
-130	1.00E+06
-140	1.00E+07

Phase noise, $\mathcal{L}(f)$,

$$f_c = \frac{f_{baud}}{128} = \sim 469.83 \text{ MHz}$$

The phase noise mask does not apply to spurs, but to broadband phase noise only. Spurs are considered separately as per 11.2.3.

11.2.3 Tx clock maximum total integrated RMS phase jitter

rms random jitter:

$$\sigma_{rj} = \frac{1}{2\pi f_c}\sqrt{2 \cdot \int_{f_1}^{f_2} 10^{\frac{\mathcal{L}(f)}{10}} df}$$

rms periodic jitter (spurs):

$$\sigma_{pj,i} = \frac{1}{\sqrt{2}\pi f_c} \cdot 10^{\frac{s_i}{20}}$$

Where:

$\mathrm{f_1} = 10\mathrm{kHz}$,
$\mathrm{f_2} = 10\mathrm{MHz}$,
$\mathrm{f_c} = \frac{\mathrm{f_{baud}}}{128} = \sim 469.83\mathrm{MHz}$
$\mathcal{L}(\mathrm{f}) = \text{phase noise (PN)}$
$s_i = \text{individual spur in [dBc]}$

rms total jitter:

$$\sigma_{tj} = \sqrt{{\sigma_{rj}}^2 + \sum_{i=1}^{N} {\sigma_{pj,i}}^2}$$

Where:

$\mathrm{N} = \text{total number of spurs.}$

11.3 Receiver Optical Specifications

The receiver optical tolerance specifications include margin for Tx and line impairments.

Ref.	Parameter	Mode	Min	Max	Unit	Conditions/Comments
	Modulation format	400G	DP-16QAM			
		300G	DP-8QAM			
		200G	DP-QPSK			
		100G	DP-QPSK			
	Baud rate	400G/300G/200G	60.138547 ± 20 ppm		GBd	
		100G	30.069274 ± 20 ppm			
	Post FEC BER	All	—	1E-15		Pre-FEC BER ≤ 2.0E-2
11.1.300	Frequency offset between received carrier and LO	All	–3.6	3.6	GHz	
11.1.310	Input power range	400G	–12	0	dBm	Signal power of the channel for the OSNR tolerance in 11.1.330.
		300G	–15	0		
		200G	–18	0		
		100G	–18	0		
11.1.330	OSNR tolerance	400G	—	24	dB/0.1 nm	At OFEC threshold. Referenced to an optical bandwidth of 0.1 nm at 193.7 THz or 12.5 GHz.
		300G	—	21		
		200G	—	16		
		100G	—	12.5		
11.1.340	Optical return loss	All	20	—	dB	At Rx connector input.
11.1.341	CD tolerance	400G	20,000	—	ps/nm	Tolerance to CD with ≤ 0.5 dB penalty to OSNR sensitivity when change in SOP is ≤ 1 rad/ms.
		300G	40,000	—		
		200G	50,000	—		
		100G	100,000	—		
11.1.342	CD OSNR tolerance penalty	All	—	0.5	dB	OSNR penalty due to chromatic dispersion.
11.1.350	PMD (avg) tolerance	400G	20	—	ps	Min tolerance limits includes the transmitter maximum X-Y skew. Tolerance to PMD with ≤ 0.5 dB penalty to OSNR sensitivity when change in SOP is ≤ 1 rad/ms. PMD (avg) is equivalent to DGDmean. DGDmax occurs when SOPMD = 0 ps^2. Due to the statistical nature of PMD the DGDmax to DGDmean Ratio is calculated at 3.3 (4.1 x 10-6 probability that DGD being greater than DGDmax).
		300G	25	—		
		200G	25	—		
		100G	30	—		

Ref.	Parameter	Mode	Min	Max	Unit	Conditions/Comments
11.1.351	Peak PDL tolerance	All	3.0	—	dB	Tolerance to peak PDL with ≤ 1.3 dB additional OSNR penalty when change in SOP is ≤ 1 rad/ms.
			3.5	—		Tolerance to peak PDL with ≤ 1.8 dB additional OSNR penalty when change in SOP is ≤ 1 rad/ms.
11.1.352	Tolerance to change in SOP	All	50	—	krad/s	With ≤ 0.5 dB additional OSNR penalty over all PMD and PDL values.
11.1.353	Optical input power transient tolerance	All	–2	2	dB	With ≤ 0.5 dB additional OSNR penalty over all PMD and PDL values.
11.1.354	Adjacent-channel crosstalk OSNR tolerance penalty	All	—	1	dB	OSNR tolerance penalty due to crosstalk interference from neighboring channels. Back-to-back through a DWDM link that conforms to the worst-case specifications of Section 11.1 and with characteristics equivalent to Section 13.
11.1.355	Intra-channel filtering penalty	All	—	0.5	dB	Due to the filtering effects of Mux/Demux in 75 GHz grid.

Table 11-5: Rx optical specifications

11.4 Optical Parameter Definitions

11.4.1 Receiver Optical Signal-to-noise Ratio Tolerance

The receiver OSNR tolerance is defined as the minimum value of OSNR (referred to 0.1 nm @193.7 THz or 12.5 GHz) that can be tolerated while maintaining the maximum BER of the application. This must be met for all powers between the maximum and minimum mean receive input power with a worst-case transmitter in a back-to-back configuration.

The receiver OSNR tolerance does not have to be met in the presence of chromatic dispersion, non-linear effects, reflections from the optical path, PMD, and PDL or optical crosstalk. These effects are specified separately but contribute to total optical path OSNR penalty.

System integrators need to account for these path penalties when evaluating network performance.

11.4.2 Out-of-Band OSNR (OOB OSNR)

Out-of-Band OSNR (OOB OSNR) is the ratio of the peak transmitter power to the integrated power outside the transmitter spectral excursion. The spectral resolution of the measurement shall be better than the maximum spectral width of the peak.

11.4.3 Differential Group Delay (DGD)

Differential group delay (DGD) is the time difference between the fractions of an optical signal transmitted in the two principal states of polarization. For distances greater than several kilometers, and assuming random (strong) polarization mode coupling, DGD in a fiber can be statistically modelled as having a Maxwellian distribution.

Due to the statistical nature of polarization mode dispersion (PMD), the relationship between maximum instantaneous DGD and mean DGD can only be defined probabilistically. The probability of the instantaneous DGD exceeding any given value can be inferred from its Maxwellian statistics.

For purposes of this specification the ratio of maximum instantaneous DGD to mean DGD is defined as 3.3, corresponding to the probability of exceeding the maximum DGD 4.1×10^{-6}.

11.4.4 Optical return loss at S_S

Reflections are caused by refractive index discontinuities along the optical path. If not controlled, they can degrade system performance through their disturbing effect on the operation of the optical source, or through multiple reflections which lead to interferometric noise at the receiver. Reflections from the optical path are controlled by specifying the:

- minimum optical return loss of the cable plant at the source reference point (S_s), including any connectors; and
- maximum discrete reflectance between source reference point (S_s) and receive reference point (R_s)

Reflectance denotes the reflection from any single discrete reflection point, whereas the optical return loss is the ratio of the incident optical power to the total returned optical power from the entire fiber including both discrete reflections and distributed backscattering such as Rayleigh scattering.

11.4.5 Discrete reflectance between S_S and R_S

Optical reflectance is defined to be the ratio of the reflected optical power present at a point, to the optical power incident to that point. The maximum number of connectors or other discrete reflection points which may be included in the optical path must be such as to allow the specified overall optical return loss to be achieved.

11.4.6 Polarization Dependent Loss (PDL)

The polarization dependent loss (PDL) is the difference (in dB) between the maximum and minimum values of the channel insertion loss (or gain) of the DWDM link from point S_s to R_s due to a variation of the State of Polarization (SOP) over all state of polarizations.

11.4.7 Polarization rotation speed

The polarization rotation speed is the rate of rotation in Stokes space of the two polarizations of the optical signal at point R_s measured in krad/s.

11.4.8 I-Q offset

I-Q offset is measured separately on each polarization and is calculated using the following formula:

$$P_{excess} = \frac{\mathrm{I}_{\mathrm{mean}}^2 + \mathrm{Q}_{\mathrm{mean}}^2}{\mathrm{P}_{\mathrm{Signal}}}$$

$$IQ_{offset} = 10\log_{10}(\mathrm{P}_{\mathrm{excess}})$$

Instantaneous I-Q offset is measured with an averaging period ≤ 1 µs to be consistent with the timescales of receiver DSP operations.

11.4.9 Mux/Demux Filter Shape

Optical multiplexer and optical demultiplexer components for 75 GHz grid spaced applications are required to have each channel centered on the relevant channel frequency and to have a filter shape that controls crosstalk between adjacent channels and the channel of interest. The filter characteristics listed in Table 13-1 items 11.1.163a through 11.1.163q, can be met by a 3rd-order Super-Gaussian filter as described by:

$$|\boldsymbol{H(f)}|^{\mathbf{2}} = \boldsymbol{exp}\left[-\ln(2) \times \left(\frac{2(f-f_0)}{B}\right)^{6}\right] \qquad \textbf{11-1}$$

This filter is a reference shape that can be used to describe mathematically the filter roll-off characteristics. No real filter will perfectly match this mathematical formula.

11.4.10 Tx spectral masks

Compliant transmitters on a 75 GHz grid are required to limit spectral content by applying minimum and maximum masks to the spectrum acquired using an optical spectrum analyzer. The spectral masks at zero frequency shift relative to the transmitter center frequency are approximated by a root-raised-cosine (RRC) roll-off factor of 0.4 for the upper limit mask, and 0.05 for the lower limit mask.

The masks are illustrated at baseband frequency, relative to the average measured power from the transmitter over a +/- 10 GHz window (excluding DC frequency). Four piece-wise linear lines define the upper mask in Figure 11-3, with the 3 lower points falling on a RRC curve with a 0.4 roll-off factor (shown in blue). Three piece-wise linear lines

define the lower mask in Figure 11-3, with the middle point falling on an RRC curve with a 0.05 roll-off factor (in green).

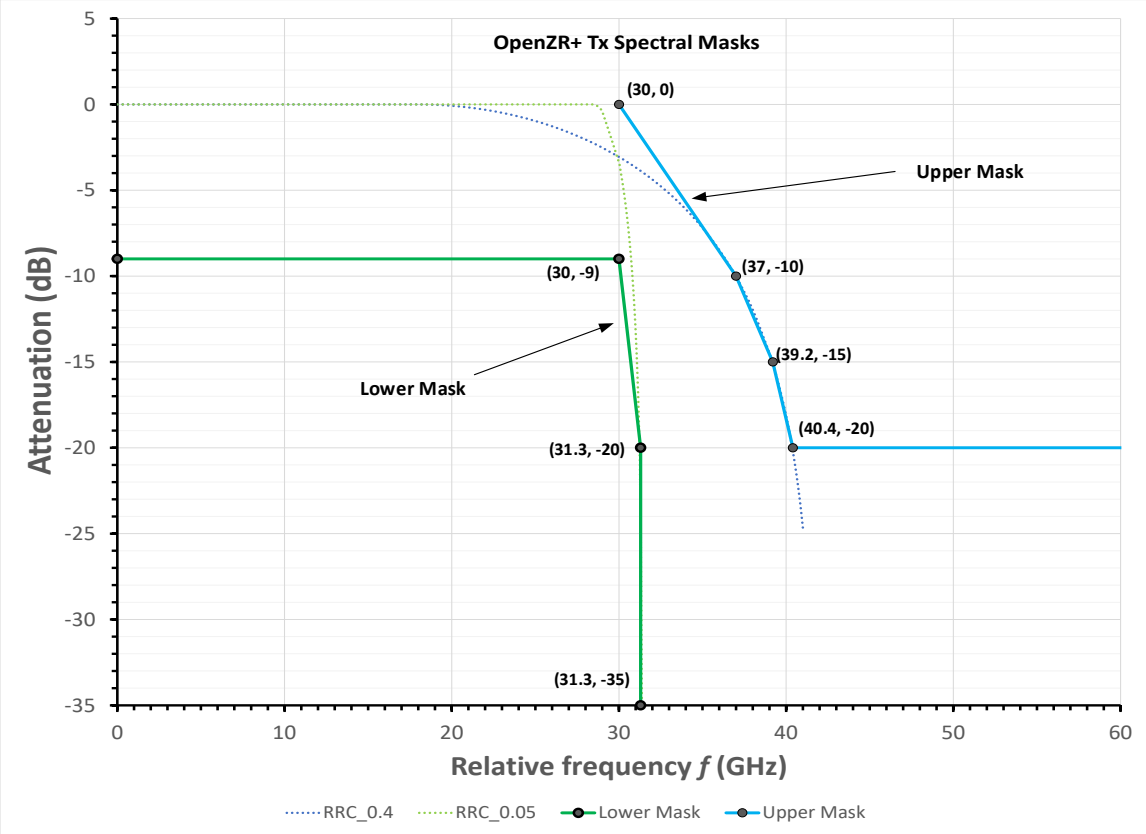


Figure 11-3 Transmit spectral masks (max and min)

12 Appendix - Host interfaces (informative)

An OpenZR+ Transponder/Muxponder may support the following host interface protocols:

Ethernet:

- 400GBASE-R
- 200GBASE-R
- 100GBASE-R

The Host/Client interface signaling is expected to conform to existing protocol standards (IEEE 802.3™-2018) and operate over standard physical layer interface(s).

12.1 400GE Clients

If the host/client signal is 400GE, then it can be multiplexed into a ZR400 frame for transmission. The required and optional (O) Ethernet physical layer clauses associated with 400GE clients are listed in Table 12-1.

Table 12-1 Ethernet physical layer clauses associated with 400GE client signals

Associated clause	ZR400-OFEC-16QAM
117—RS	Required
117—400GMII	O
118—400GMII Extender	O
119—PCS for 400GBASE-R	Required
120—PMA for 400GBASE-R	Required
120B—Chip-to-chip 400GAUI-16	O
120C—Chip-to-module 400GAUI-16	O
120D—Chip-to-chip 400GAUI-8	O
120E—Chip-to-module 400GAUI-8	O

The client logic for 400GE is shown in Figure 12-1. The block diagram shows the required operations between a 400GE PMA sublayer and the GMP mapping sublayer of the OpenZR+ architecture.

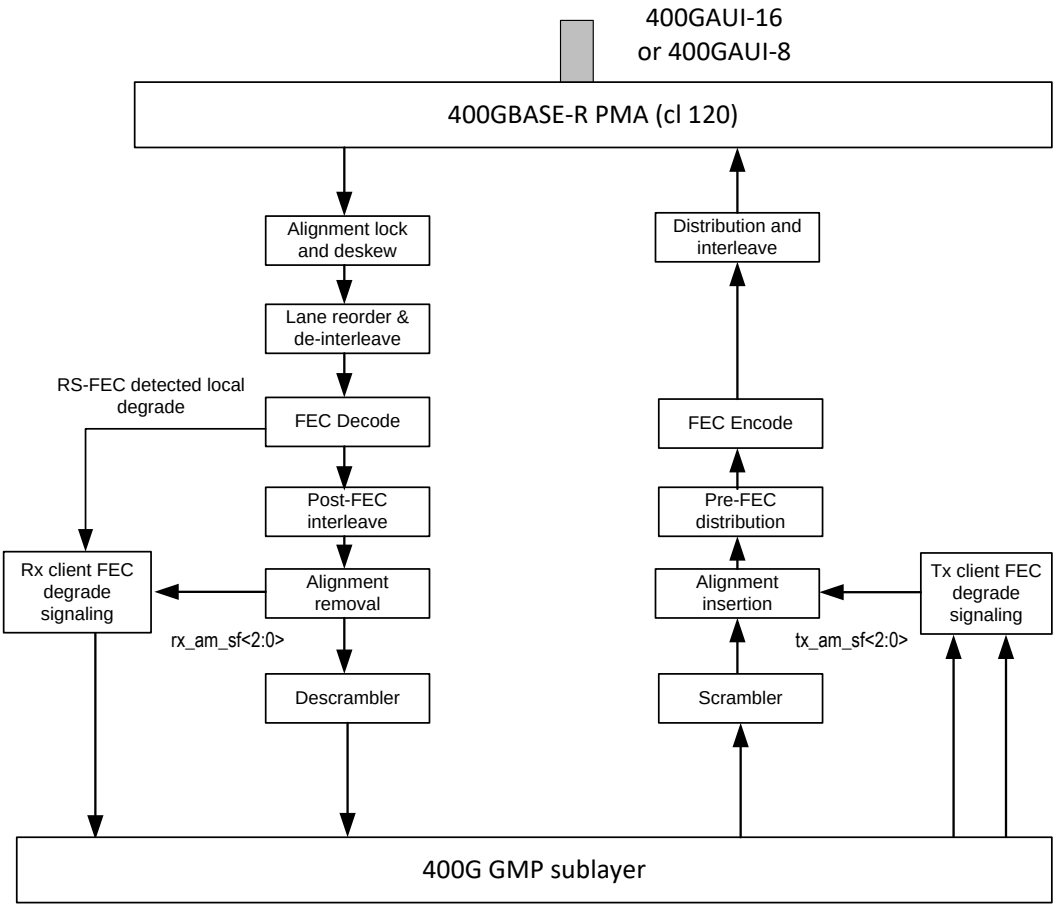


Figure 12-1 400GE client logic block diagram

12.2 200GE Clients

If the host/client signal is 200GE, then it may be multiplexed into a ZR200 or a ZR400 frame for transmission. The required and optional (O) Ethernet physical layer clauses associated with 200GE clients are listed in Table 12-2.

Table 12-2 Ethernet physical layer clauses associated with 200GE client signals

Associated clause	ZR400-OFEC-16QAM	ZR300-OFEC-8QAM	ZR200-OFEC-QPSK
117—RS	Required (up to 2)	N/A	Required
117—200GMII	O		O
118—200GMII Extender	O		O
119—PCS for 200GBASE-R	Required (up to 2)		Required
120—PMA for 200GBASE-R	Required (up to 2)		Required
120B—Chip-to-chip 200GAUI-8	O		O
120C—Chip-to-module 200GAUI-8	O		O
120D—Chip-to-chip 200GAUI-4	O		O
120E—Chip-to-module 200GAUI-4	O		O

The client logic for 200GE is shown in Figure 12-2. The block diagram shows the required operations between a 400GE PMA sublayer and the GMP mapping sublayer of the OpenZR+ architecture.

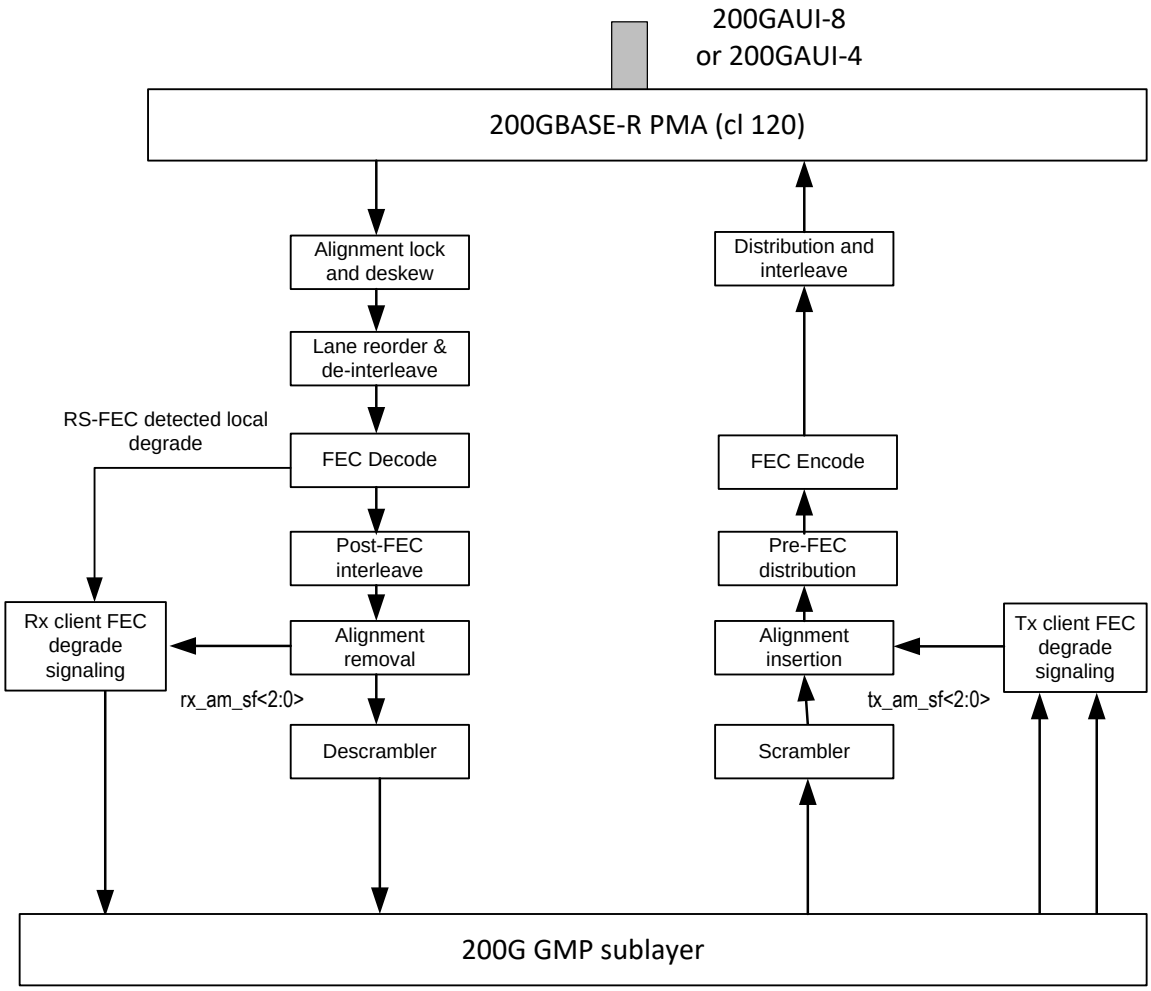


Figure 12-2 200GE client logic block diagram

12.3 100GE Clients

If the host/client signal is 100GE, then it may be multiplexed into a ZR100, ZR200, ZR300 or ZR400 frame for transmission. The required and optional (O) Ethernet physical layer clauses associated with 100GE clients are listed in Table 12-3.

Some 100GE clients may be 64b/66b encoded and will require transcoding to 256b/257b blocks before conversion to a ZR100 frame. Other 100GE clients that implement clause 91 RS-FEC will be 256b/257b encoded and will require FEC decoding before conversion to a ZR100 frame. All 100GE clients will have 8-byte alignment markers on 20 virtual PCS lanes. These will be removed by OpenZR+ implementations and replaced by 4 x 120b alignment markers in the ZR100 frame as described in 5.4.2.

Table 12-3 Ethernet physical layer clauses associated with 100GE client signals

Associated clause	ZR400-OFEC-16QAM	ZR300-OFEC-8QAM	ZR200-OFEC-QPSK	ZR100-OFEC-QPSK
81—RS	Required (up to 4)	Required (up to 3)	Required (up to 2)	Required
81—100GMII	O	O	O	O
82—PCS	Required (up to 4)	Required (up to 3)	Required (up to 2)	Required
91—RS-FEC RS(514,528)[a]	O	O	O	O
91—RS-FEC RS(514,544)[b]	O	O	O	O
83—100GBASE-R PMA[a]	O	O	O	O
135—100GBASE-P PMA[b]	O	O	O	O
83D—CAUI-4 C2C[a]	O	O	O	O
83E—CAUI-4 C2M[a]	O	O	O	O
135D—100GAUI-4 C2C[b]	O	O	O	O
135E—100GAUI-4 C2M[b]	O	O	O	O
135F—100GAUI-2 C2C[b]	O	O	O	O
135G—100GAUI-2 C2M[b]	O	O	O	O

Notes: [a]If CAUI-4 C2C or C2M are present then clause 83 100GBASE-R PMA is required and clause 91 RS-FEC with RS(514,528) is optional.
[b]If 100GAUI-4 C2C, 100GAUI-4 C2M, 100GAUI-2 C2C or 100GAUI-2 C2M are present then clause 135 100GBASE-P PMA is required and clause 91 RS-FEC with RS (514,544) is required.

The client logic for a 100GE client implementing clause 91 RS-FEC is shown in Figure 12-3. The block diagram shows the required operations between a 100GE PMA sublayer and the 100G GMP mapping sublayer of the OpenZR+ architecture.

The client logic for a 100GE client without FEC is shown in Figure 12-3. The block diagram shows the required operations between a 100GE PMA sublayer and the 100G GMP mapping sublayer of the OpenZR+ architecture.

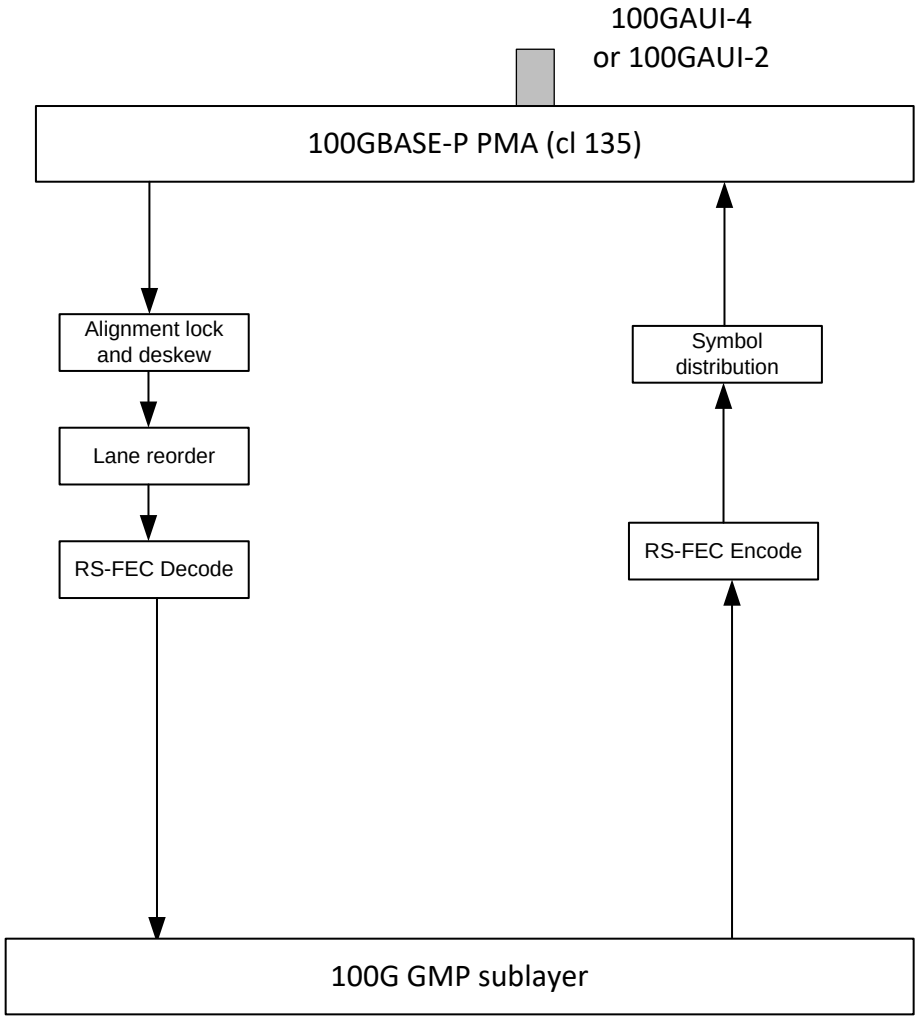


Figure 12-3 100GE with RS-FEC logic block diagram

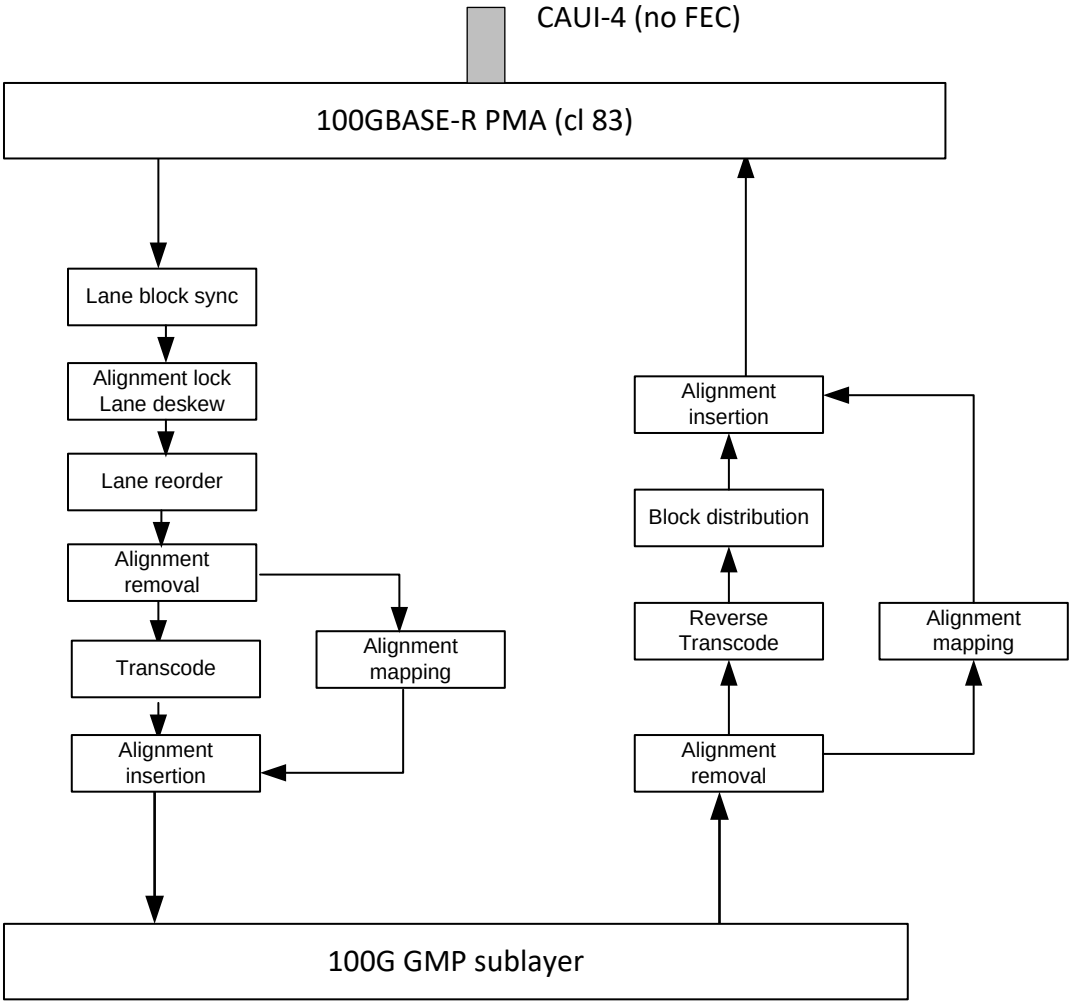


Figure 12-4 100GE client without FEC logic block diagram

12.4 Client signal processing

OpenZR+ implementations provide the required processing between incoming and outgoing client signals and the 400ZR, 200ZR or 100ZR formatted frames detailed in sections 3.2, 3.4 and 3.5. The required functions include:

PMA processing

- Per-input-lane clock and data recovery
- Bit-level multiplexing
- Clock generation
- Signal drivers
- Tolerate skew variation
- Optionally provide loopback and test-pattern generation and checking

PCS processing

- Encoding (decoding) data octets to (from) 66-bit blocks (64B/66B) [100GE clients without RS-FEC only].
- Transcoding from 66-bit blocks to (from) 257-bit blocks [100GE clients without RS-FEC only].

- Insert (remove) alignment markers
- Reed-Solomon encoding (decoding) the 257-bit blocks.
- Transferring encoded data to (from) the PMA sublayer including alignment lock, lane deskew, lane reorder and de-interleave in the egress direction.

13 Appendix – Example link characteristics for 75 GHz grid spacing

In addition to the link parameters specified in Table 11-1, for operation on a 75 GHz grid, there needs to be filtering between channels to achieve sufficient crosstalk control. Figure 13-1 is an example implementation with Mux/DMux characteristics as in Figure 13-2 and Figure 13-3. The parameter values are in Table 13-1.

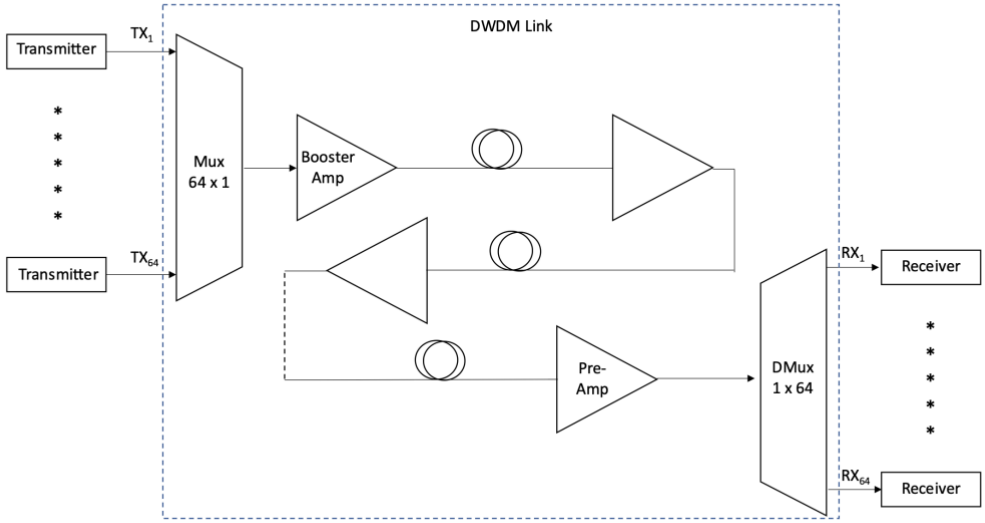


Figure 13-1 Example DWDM Link for 75 GHz grid spacing

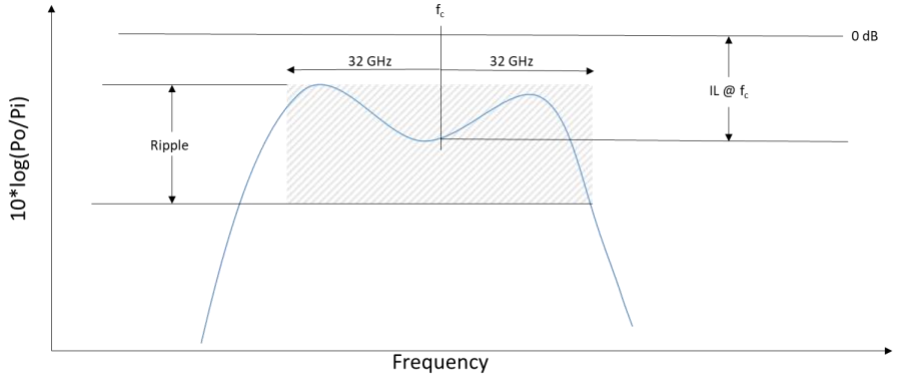


Figure 13-2 Definition of insertion loss and ripple for Mux/Demux filters

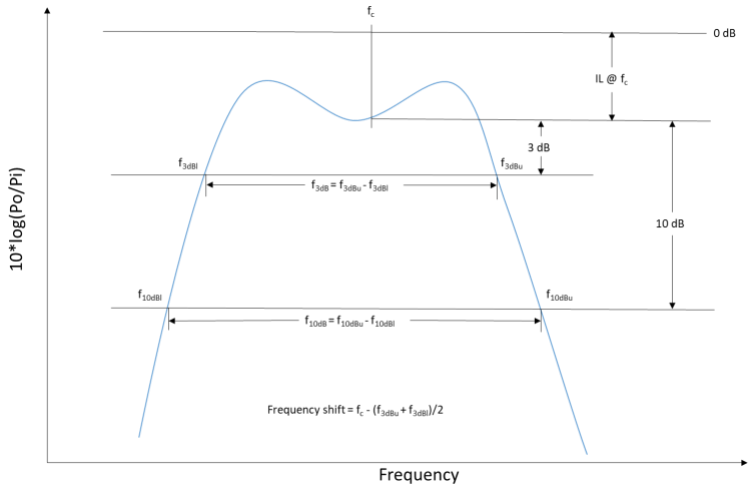


Figure 13-3 Definition of Mux/Demux filter characteristics

Ref.	Parameter	Mode	Min	Max	Unit	Conditions / Comments
11.1.163	Optical multiplexer or demultiplexer characteristics	All				See 11.1.163a through 11.1.163q for individual required characteristics
11.1.163a	Filter shape for single Mux or Demux	All				3rd-order Super-Gaussian. See definition at 11.4.9.
11.1.163b	3 dB bandwidth Mux, (f_{3dB})	All	70	76	GHz	See Figure 13-3
11.1.163c	3 dB bandwidth Demux, (f_{3dB})	All	70	76	GHz	See Figure 13-3
11.1.163d	10 dB bandwidth Mux, (f_{10dB})	All	85	94	GHz	See Figure 13-3
11.1.163e	10 dB bandwidth Demux, (f_{10dB})	All	85	94	GHz	See Figure 13-3
11.1.163f	Insertion loss Mux, (IL)	All	—	6.5	dB	See Figure 13-2
11.1.163g	Insertion loss Demux, (IL)	All	—	6.5	dB	See Figure 13-2
11.1.163h	Insertion loss variation Mux	All	—	1.5	dB	Across all channels at center frequency
11.1.163i	Insertion loss variation Demux	All	—	1.5	dB	Across all channels at center frequency
11.1.163j	Adjacent channel isolation Mux	All	30	—	dB	With respect to center frequency
11.1.163k	Adjacent channel isolation Demux	All	30	—	dB	With respect to center frequency
11.1.163l	Non-adjacent channel isolation Mux	All	25	—	dB	With respect to center frequency
11.1.163m	Non-adjacent channel isolation Demux	All	25	—	dB	With respect to center frequency
11.1.163n	Frequency shift of Mux	All	–4	4	GHz	See Figure 13-3
11.1.163o	Frequency shift of Demux	All	–4	4	GHz	See Figure 13-3
11.1.163p	Ripple of Mux	All	—	2.5	dB	See Figure 13-3
11.1.163q	Ripple of Demux	All	—	2.5	dB	See Figure 13-3

Table 13-1 Example Mux/Demux characteristics for 75 GHz grid operation

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